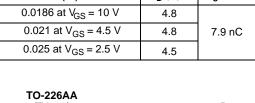
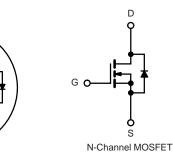


N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A) ^a	Q _g (Typ.)	
	0.0186 at V _{GS} = 10 V	4.8		
20	0.021 at V _{GS} = 4.5 V	4.8	7.9 nC	
	0.025 at V _{GS} = 2.5 V	4.5		



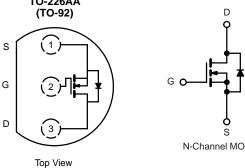


FEATURES

- · Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested

APPLICATIONS

· Load Switch



ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unles	ss otherwise no	oted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	20	V	
Gate-Source Voltage		V_{GS}	± 12	V	
	T _C = 25 °C		4.8 ^a		
Continuous Drain Current /T 450 °C\8	T _C = 70 °C	1	4.5 ^a		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	4.8 ^{a, b, c}		
	T _A = 70 °C		4.5 ^{a, b, c}	Α	
Pulsed Drain Current		I _{DM}	20		
Continuous Source-Drain Diode Current	T _C = 25 °C	Is	4.5 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	2.9 ^{b, c}		
	T _C = 25 °C		1.9	W	
Maximum Power Dissipation	T _C = 70 °C	P _D	1.2		
Maximum Fower Dissipation	T _A = 25 °C	ט' ט	0.5 ^{b, c}		
	T _A = 70 °C		0.2 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature)			260	C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient	t ≤ 5 s	R _{thJA}	28	36	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5] 5/**	

Notes:

- a. Package limitedb. Surface Mounted on 1" x 1" FR4 board.
- c. t = 5 s.

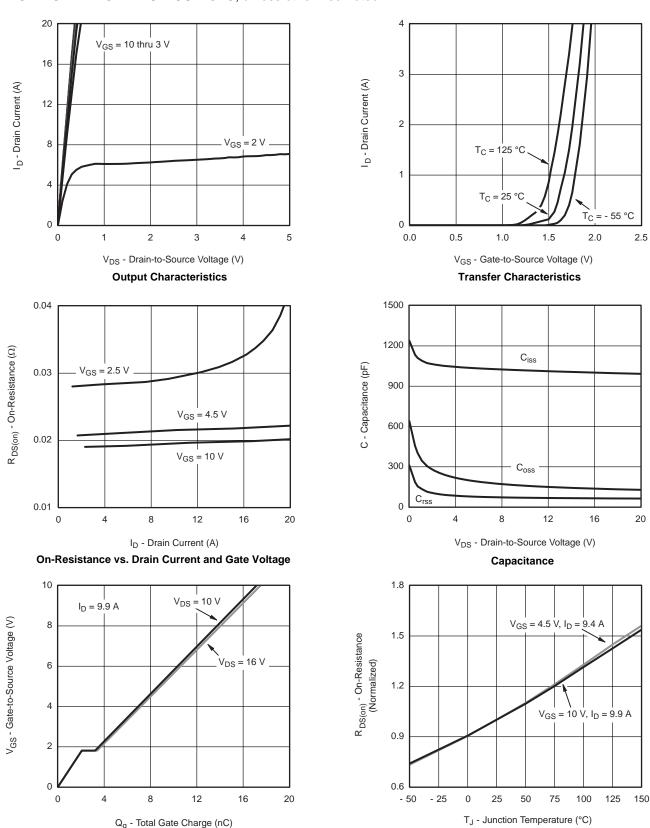
COMPLIANT



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					L		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 250A		25		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu\text{A}$		- 3.7			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.6		1.5	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current		V _{DS} = 20 V, V _{GS} = 0 V			1	.	
	I _{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 5 \text{ V}, V_{GS} = 4.5 \text{ V}$		20		Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 4.8 \text{ A}$		0.0186		†	
		V _{GS} = 4.5 V, I _D = 4.8 A		0.021		Ω	
		$V_{GS} = 2.5 \text{ V}, I_D = 4.8 \text{ A}$		0.025		1	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 4.8 A		20		S	
Dynamic ^b	<u> </u>	,			<u>I</u>		
Input Capacitance	C _{iss}			1020		pF	
Output Capacitance	C _{oss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		160			
Reverse Transfer Capacitance	C _{rss}			70			
		V _{DS} = 10 V, V _{GS} = 10 V, I _D = 4.8 A		17.5	27	+	
Total Gate Charge	Q_g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.8 A		7.9	16	nC	
Gate-Source Charge	Q_{gs}			2.1			
Gate-Drain Charge	Q_{gd}			1.1			
Gate Resistance	R_g	f = 1 MHz	0.6	3	6	Ω	
Turn-On Delay Time	t _{d(on)}			12	18		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_{L} = 1.3 \Omega$		11	17	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 3.9 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		27	41		
Fall Time	t _f			11	17		
Turn-On Delay Time	t _{d(on)}			7	14		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_{L} = 1.3 \Omega$		10	15		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 3.9 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t _f			8	16		
Drain-Source Body Diode Characterist	ics	,			<u> </u>		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.5 ^c	۸	
Pulse Diode Forward Current	I _{SM}				20	A	
Body Diode Voltage	V_{SD}	$I_S = 3.9 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			16	24	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	$I_F = 7.9 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		6	12	nC	
Reverse Recovery Fall Time	IE = 7.9 A. UI/			7		ns	
Reverse Recovery Rise Time	t _b			8			

- Notes: a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing. c. Package Limited

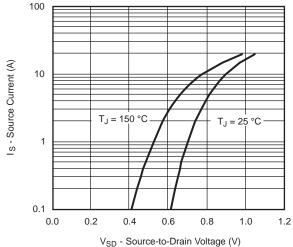




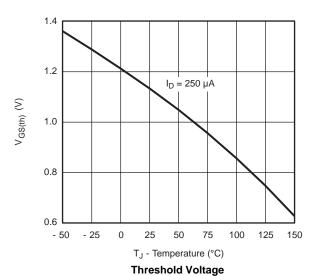
Gate Charge

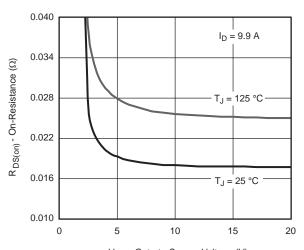
On-Resistance vs. Junction Temperature





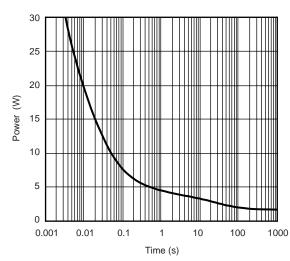
Soure-Drain Diode Forward Voltage



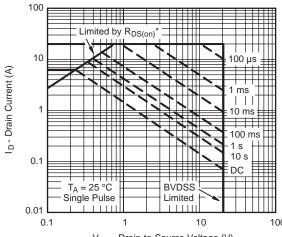


V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

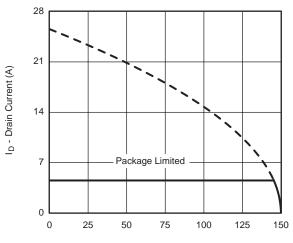


V_{DS} - Drain-to-Source Voltage (V)

* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

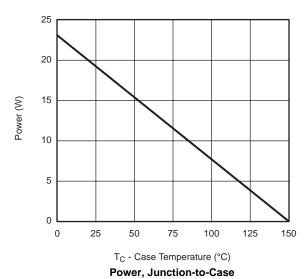
Safe Operating Area, Junction-to-Ambient

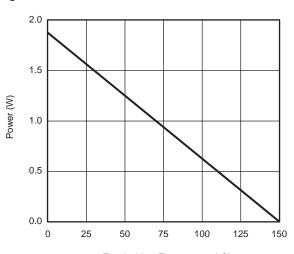




T_C - Case Temperature (°C)

Current Derating*

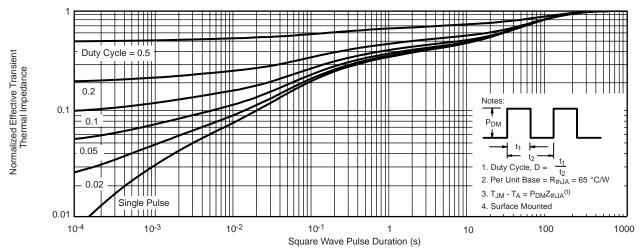




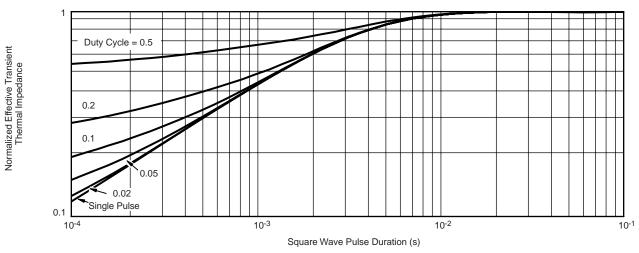
T_A - Ambient Temperature (°C) **Power, Junction-to-Ambient**

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

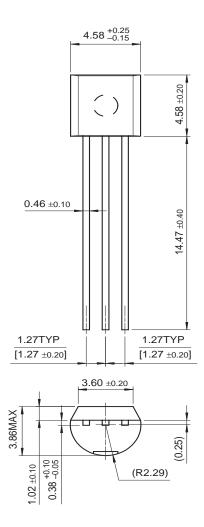


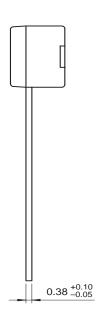
Normalized Thermal Transient Impedance, Junction-to-Case



Mechanical Dimensions

TO-92







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