

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.008 at $V_{GS} = 10$ V	30	8.4nC
	0.013 at $V_{GS} = 4.5$ V	25	

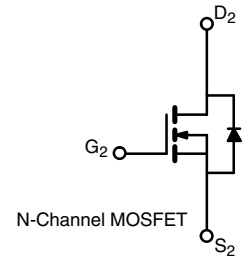
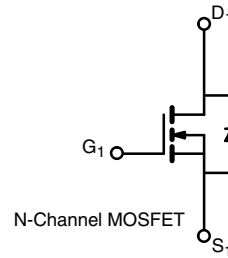
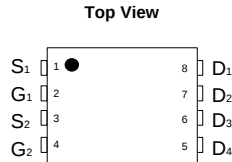
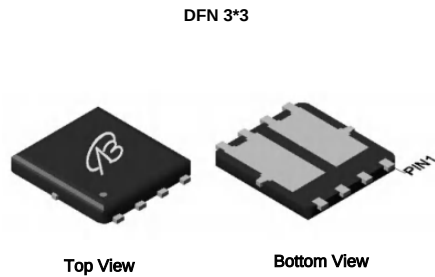
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- Optimized for High-Side Synchronous Rectifier Operation
- 100 % R_g Tested
- 100 % UIS Tested


RoHS
 COMPLIANT

APPLICATIONS

- Notebook CPU Core
- High-Side Switch



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	30	A
	$T_C = 70^\circ\text{C}$		25	
	$T_A = 25^\circ\text{C}$		15 ^{b, c}	
	$T_A = 70^\circ\text{C}$		7.5 ^{b, c}	
Pulsed Drain Current		I_{DM}	90	mJ
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	I_S	3.2	
	$T_A = 25^\circ\text{C}$		1.6 ^{b, c}	
Single Pulse Avalanche Current	$L = 0.1$ mH	I_{AS}	17	
Avalanche Energy		E_{AS}	21	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	4.1	W
	$T_C = 70^\circ\text{C}$		2.5	
	$T_A = 25^\circ\text{C}$		2.1 ^{b, c}	
	$T_A = 70^\circ\text{C}$		1.2 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ s	R_{thJA}	39	53	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	29	

Notes:

 a. Base on $T_C = 25^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

 c. $t = 10$ s.

 d. Maximum under Steady State conditions is 85°C/W .

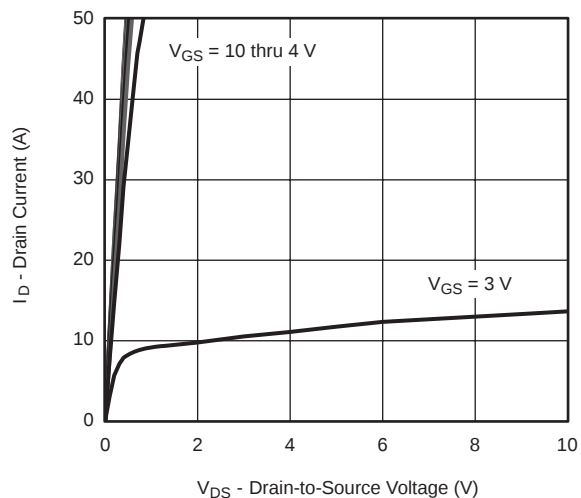
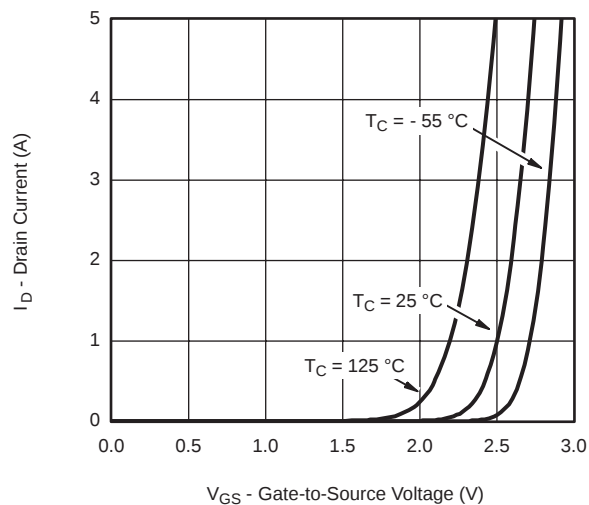
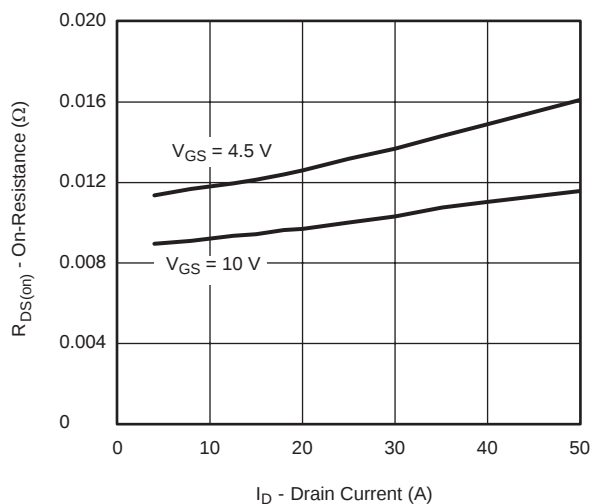
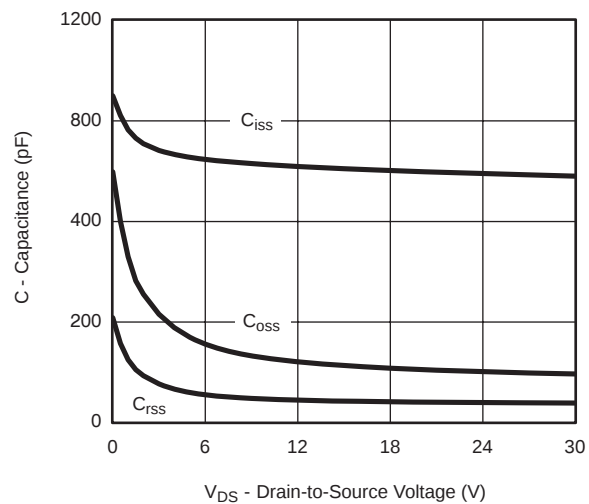
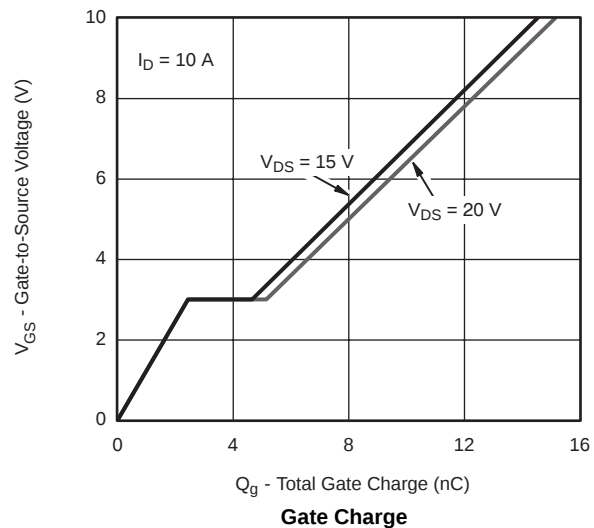
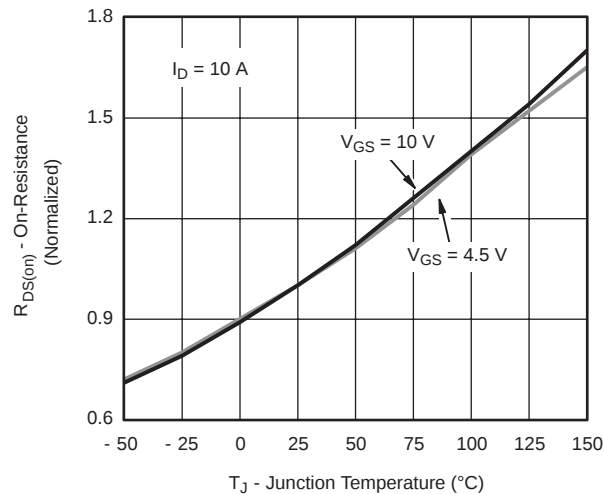
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		28		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		0.008		Ω
		V _{GS} = 4.5 V, I _D = 9 A		0.013		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		52		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1440		pF
Output Capacitance	C _{oss}			175		
Reverse Transfer Capacitance	C _{rss}			73		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A		15	23	nC
		V _{DS} = 15 V, V _{GS} = 5 V, I _D = 10 A		6.8	10.2	
Gate-Source Charge	Q _{gs}			2.5		
Gate-Drain Charge	Q _{gd}			2.3		
Gate Resistance	R _g	f = 1 MHz	0.36	1.8	3.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.4 Ω I _D ≅ 9 A, V _{GEN} = 4.5 V, R _g = 1 Ω		16	24	ns
Rise Time	t _r			12	18	
Turn-Off Delay Time	t _{d(off)}			16	24	
Fall Time	t _f			10	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.4 Ω I _D ≅ 9 A, V _{GEN} = 10 V, R _g = 1 Ω		8	16	
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			16	24	
Fall Time	t _f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			30	A
Pulse Diode Forward Current ^a	I _{SM}				90	
Body Diode Voltage	V _{SD}	I _S = 9 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 9 A, di/dt = 100 A/μs, T _J = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}			6	12	nC
Reverse Recovery Fall Time	t _a			8		ns
Reverse Recovery Rise Time	t _b			7		

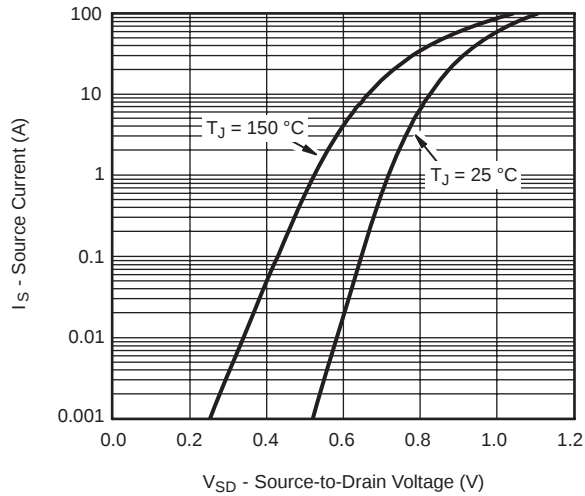
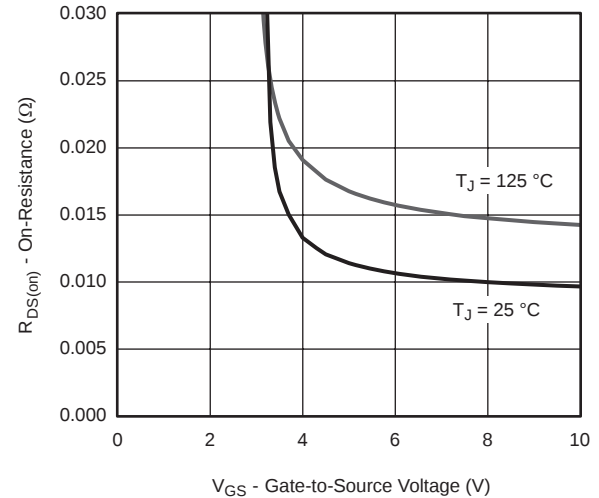
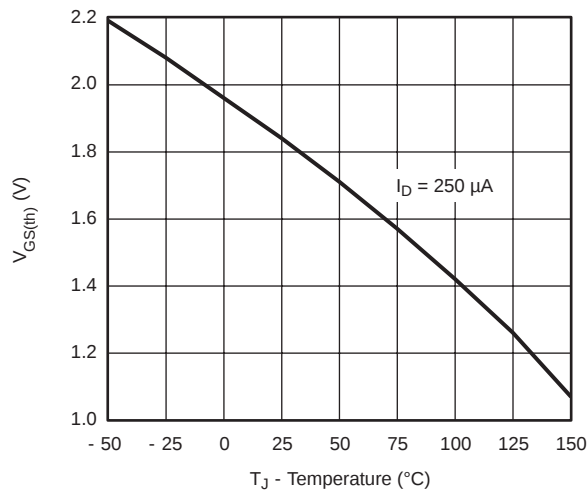
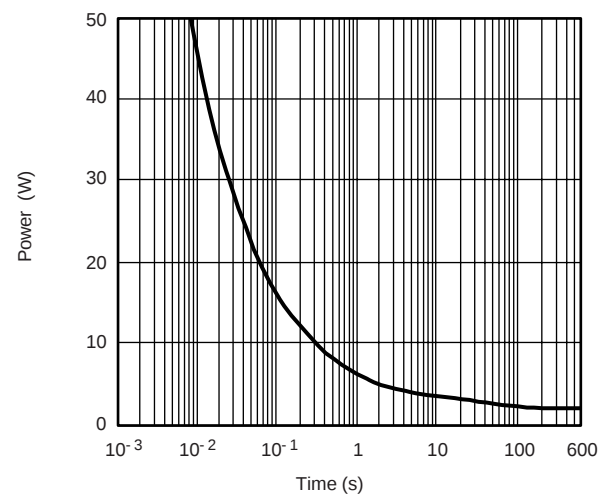
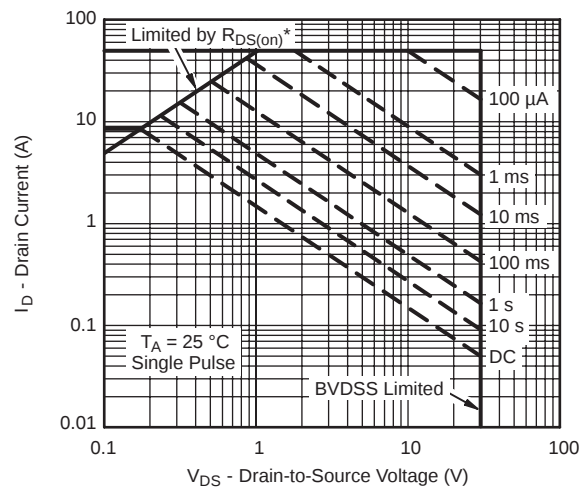
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

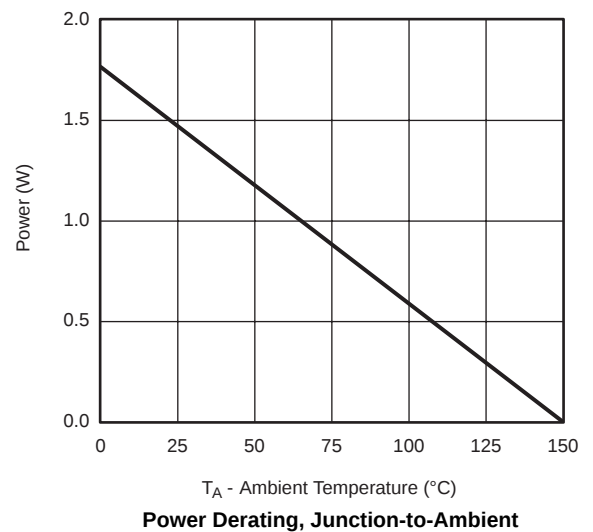
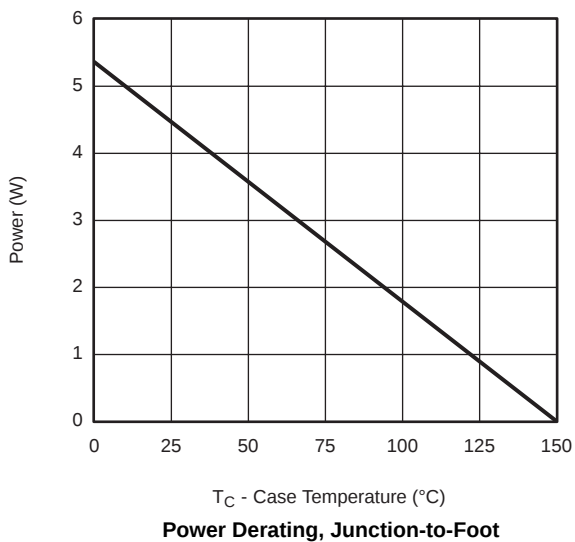
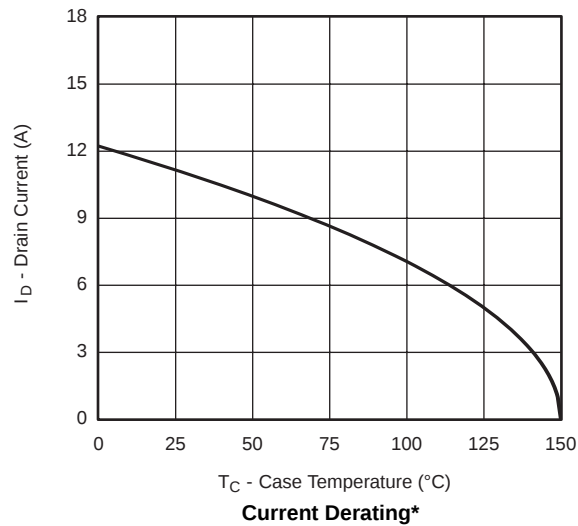
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

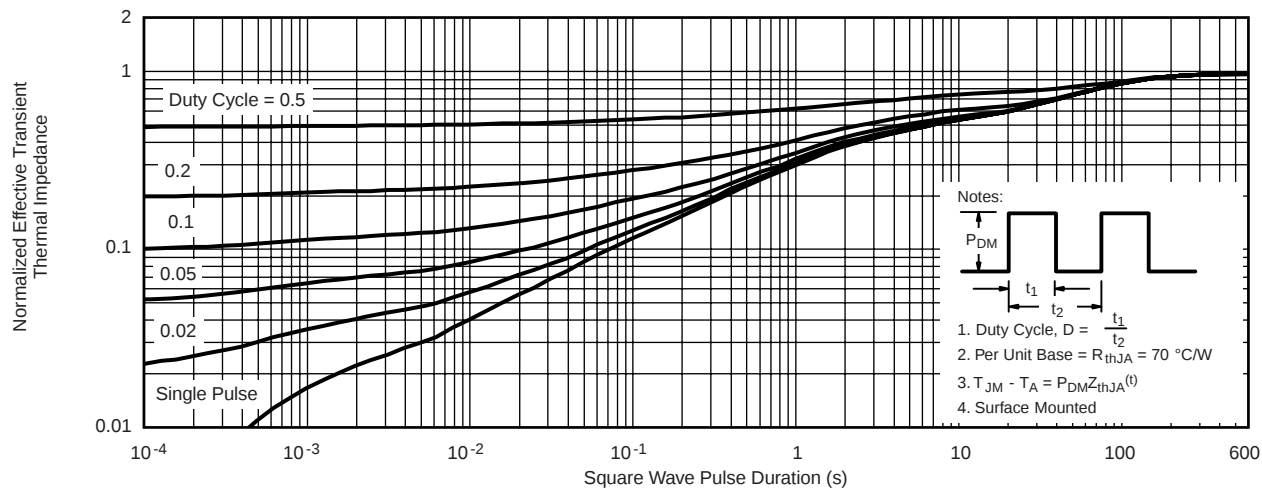
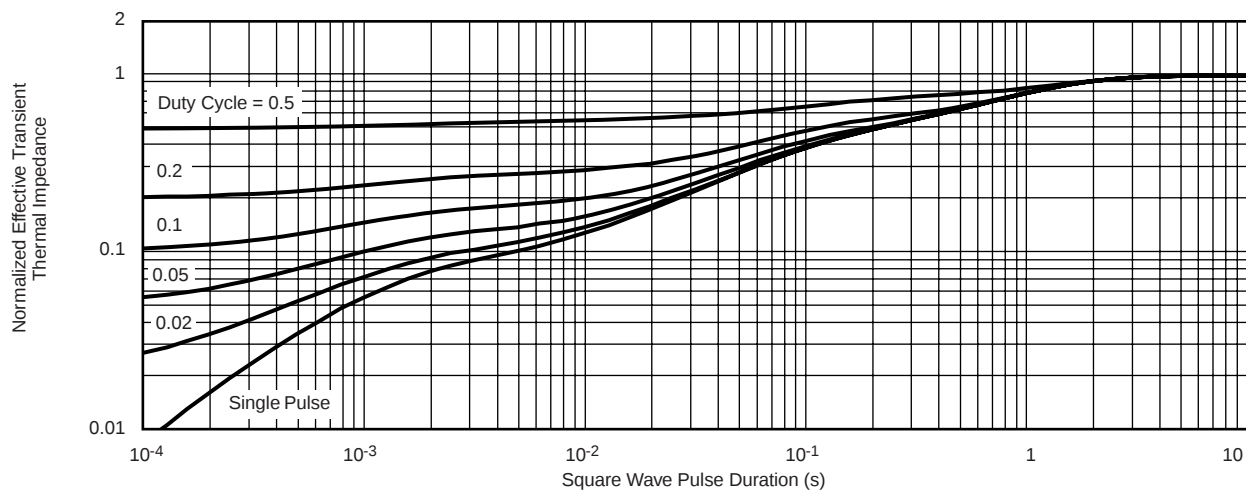
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

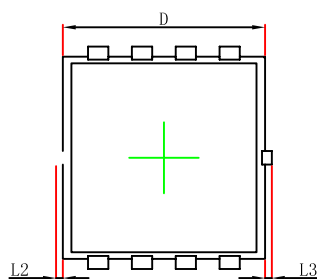
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


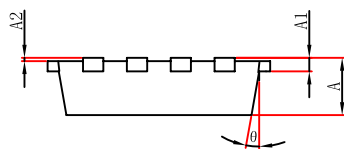
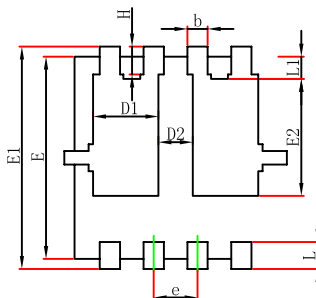
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

PDFNWB3.3×3.3-8L-B Package Outline Dimensions



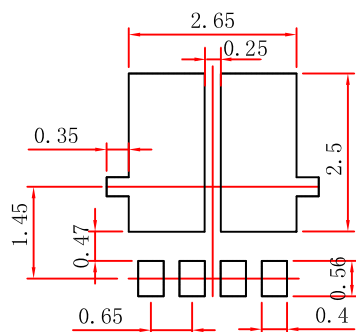
Top View
[顶视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	0.935	1.135	0.037	0.045
D2	0.280	0.480	0.011	0.019
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3×3.3-8L-B Suggested



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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