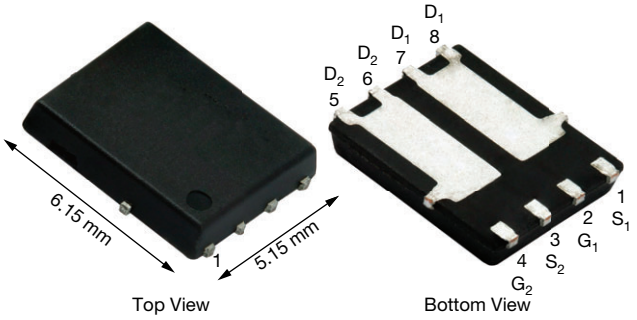
Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[e,f]	Q_g (Typ.)
- 30	0.019 at V_{GS} = - 10 V	- 30	24.6 nC
	0.021 at V_{GS}=-4.5V	- 28	

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

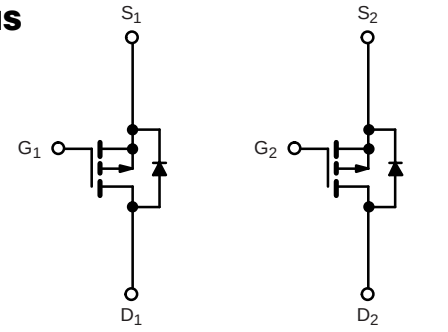
RoHS COMPLIANT
HALOGEN FREE



Top View Bottom View

APPLICATIONS

- Load Switch
- Adaptor Switch
- Notebook PC



P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 30[e]	A
	T_C = 70 °C		- 28[e]	
	T_A = 25 °C		- 16.1[a, b]	
	T_A = 70 °C		- 12.9[a, b]	
Pulsed Drain Current		I_{DM}	- 60	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 15	
	T_A = 25 °C		- 3.5[a, b]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 25	
Single-Pulse Avalanche Energy		E_{AS}	31.25	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	35.7	W
	T_C = 70 °C		22.8	
	T_A = 25 °C		4.2[a, b]	
	T_A = 70 °C		2.7[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature)[c, d]			260	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. The DFN 5x6 package is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Package limited.
f. Based on T_C = 25 °C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	t ≤ 10 s	R_{thJA}	25	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.9	3.5	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Maximum under steady state conditions is 70 °C/W.

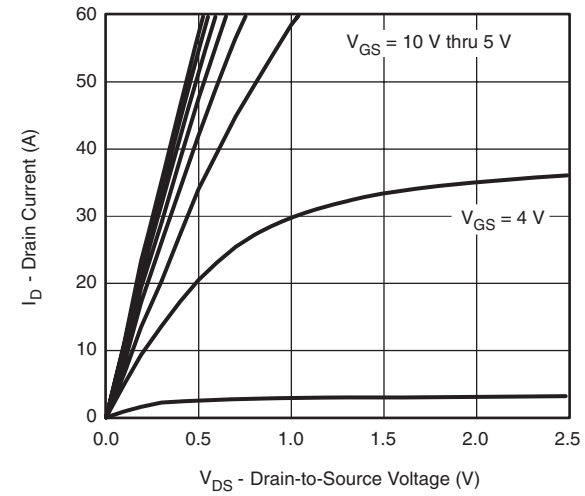
SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.2		- 2.8	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 10 V	- 3 0			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 10 A		0.0190		Ω
		V_{GS} = - 4.5 V, I_D = 10 A		0.0210		
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 12 A		37		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 15 V, V_{GS} = 0 V, f = 1 MHz		2000		pF
Output Capacitance	C_{oss}			385		
Reverse Transfer Capacitance	C_{rss}			322		
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 14.4 A		47.5	71	nC
		V_{DS} = - 15 V, V_{GS} = - 4.5 V, I_D = - 14.4 A		24.6	37	
Gate-Source Charge	Q_{gs}			7.7		
Gate-Drain Charge	Q_{gd}			12		
Gate Resistance	R_g	f = 1 MHz	0.3	1.5	3.0	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω, I_D ≅ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		50	75	ns
Rise Time	t_r			43	65	
Turn-Off DelayTime	$t_{d(off)}$			30	45	
Fall Time	t_f			14	21	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 1.5 Ω, I_D ≅ - 10 A, V_{GEN} = - 10 V, R_g = 1 Ω		14	21	
Rise Time	t_r			9	18	
Turn-Off DelayTime	$t_{d(off)}$			36	54	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 1 0	A
Pulse Diode Forward Current[a]	I_{SM}				- 3 0	
Body Diode Voltage	V_{SD}	I_F = - 10 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		31	47	ns
Body Diode Reverse Recovery Charge	Q_{rr}			30	45	nC
Reverse Recovery Fall Time	t_a			15		ns
Reverse Recovery Rise Time	t_b			16		

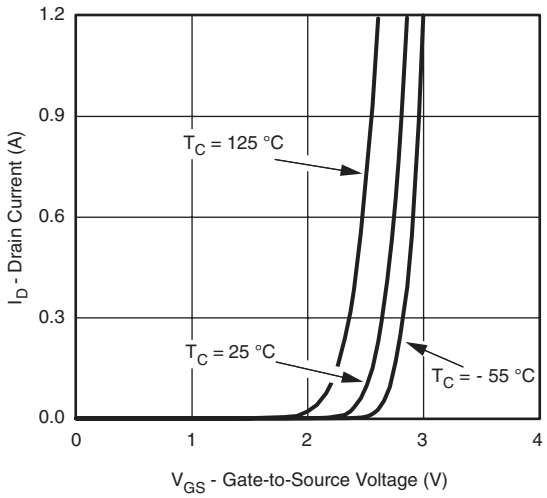
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

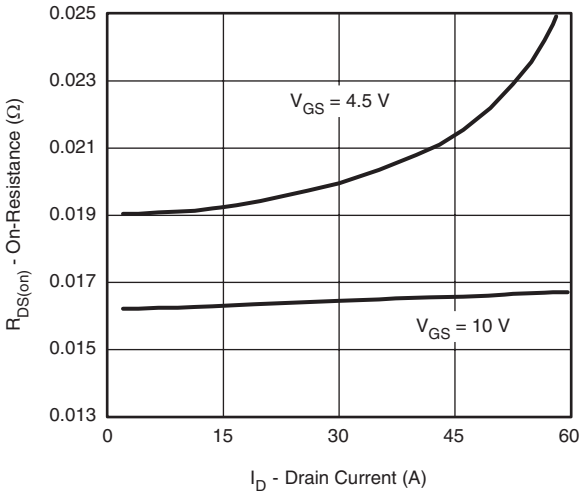
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



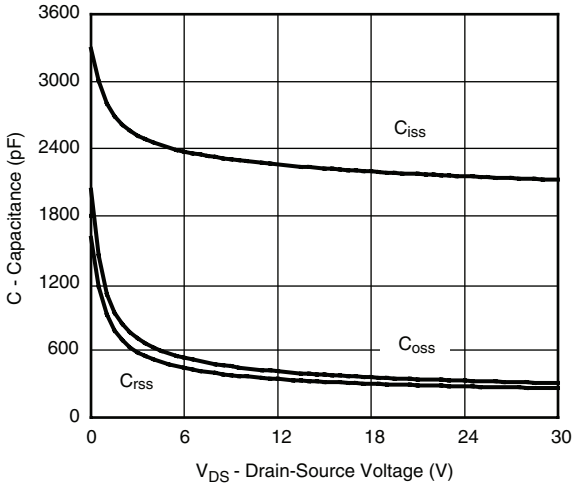
Output Characteristics



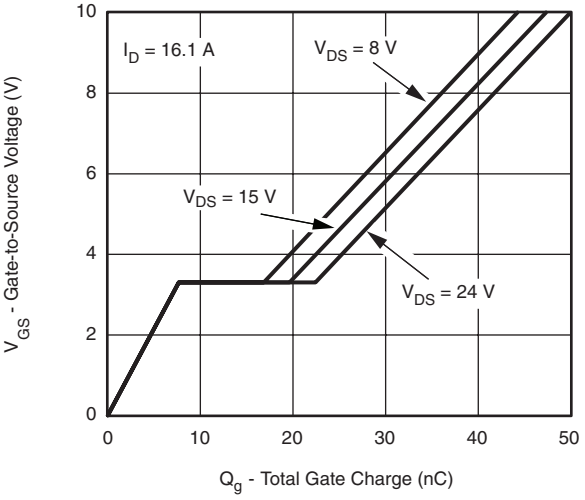
Transfer Characteristics



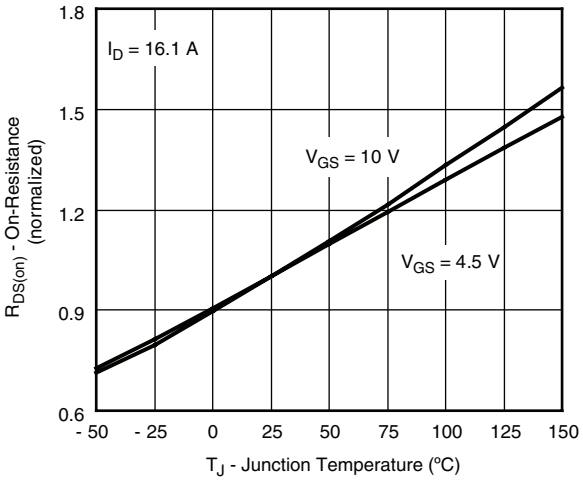
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

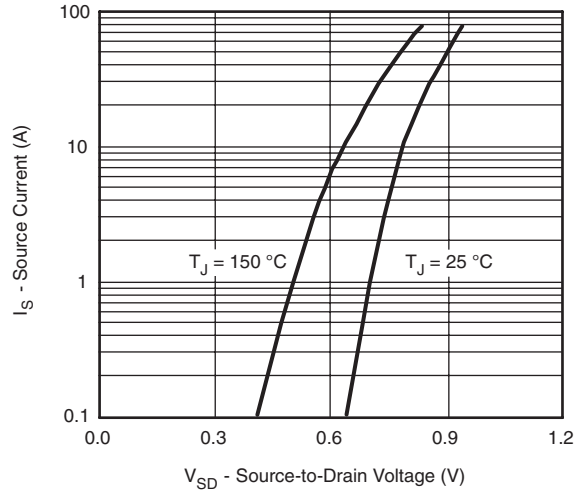


Gate Charge

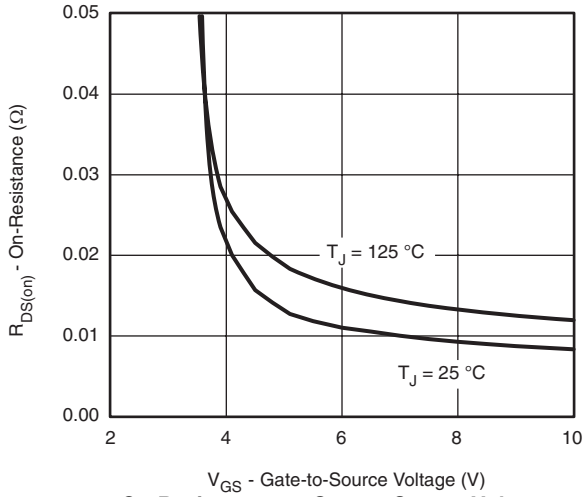


On-Resistance vs. Junction Temperature

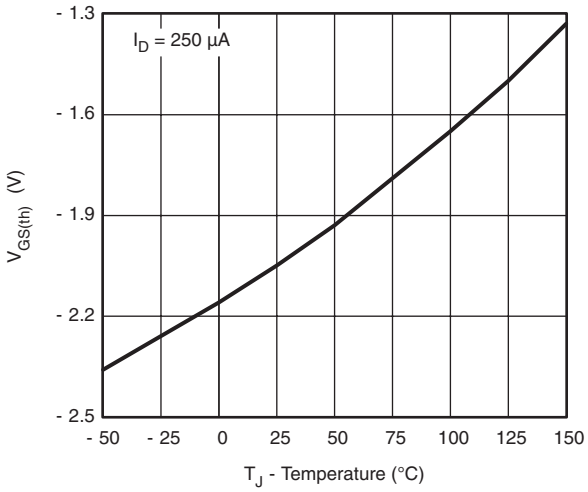
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



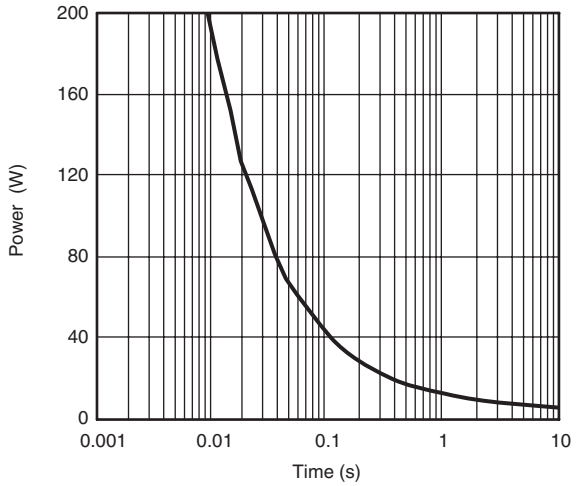
Source-Drain Diode Forward Voltage



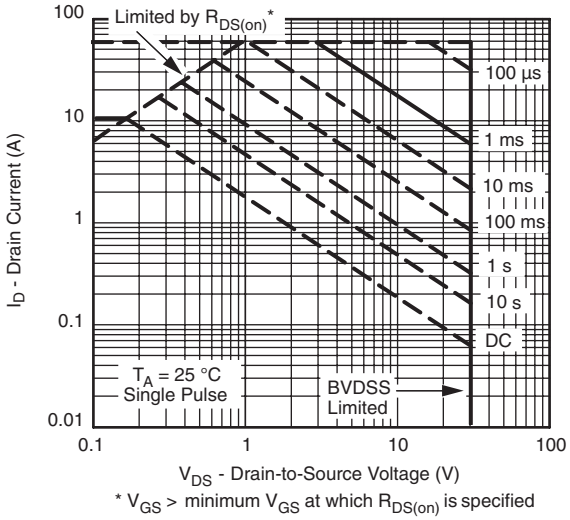
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

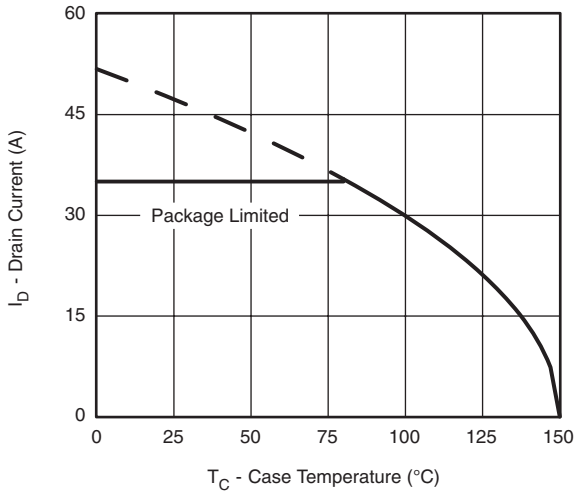


Single Pulse Power, Junction-to-Ambient

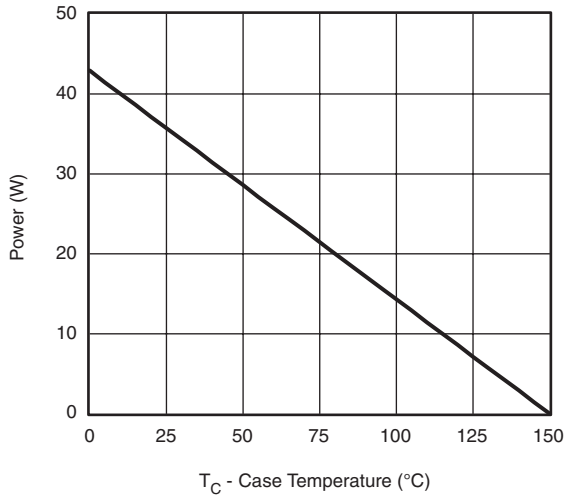


Safe Operating Area, Junction-to-Ambient

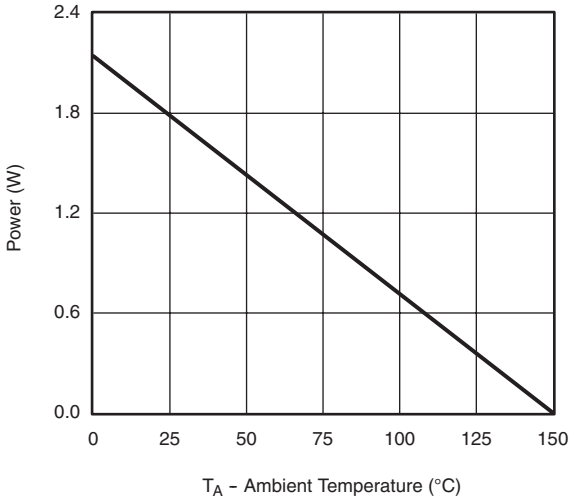
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



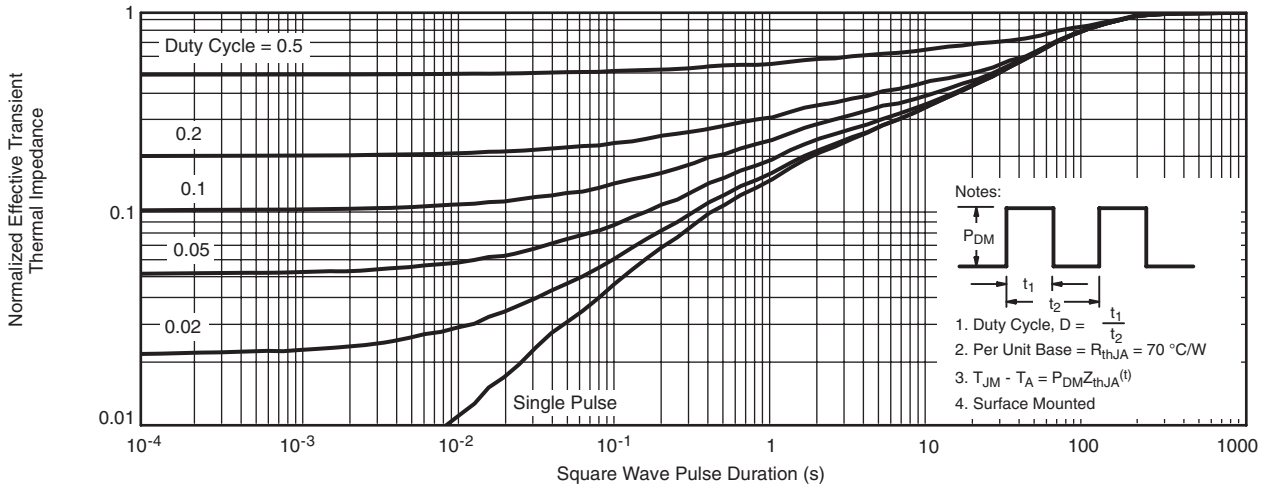
Power, Junction-to-Case



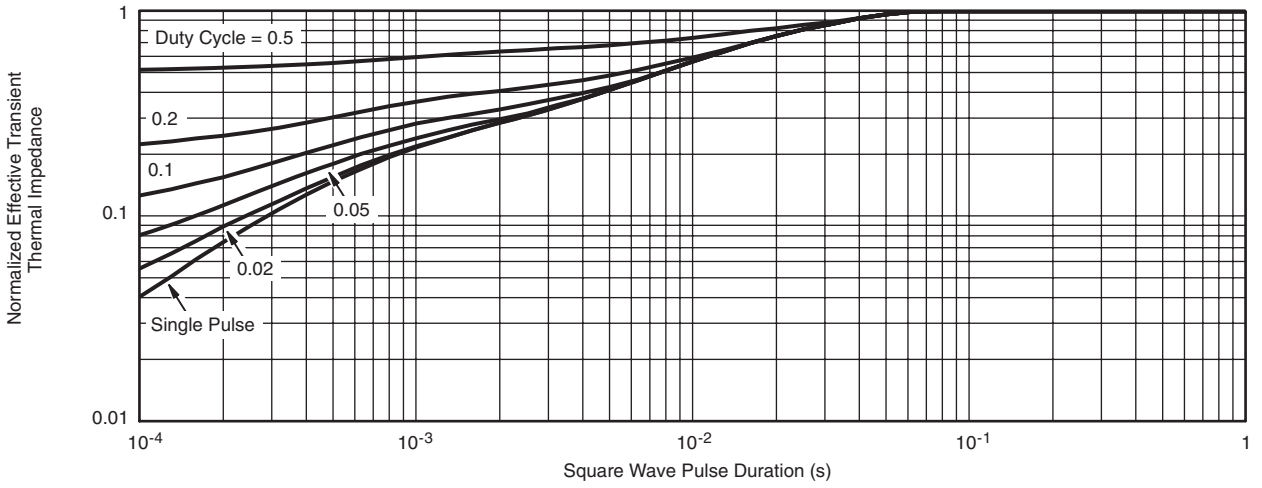
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

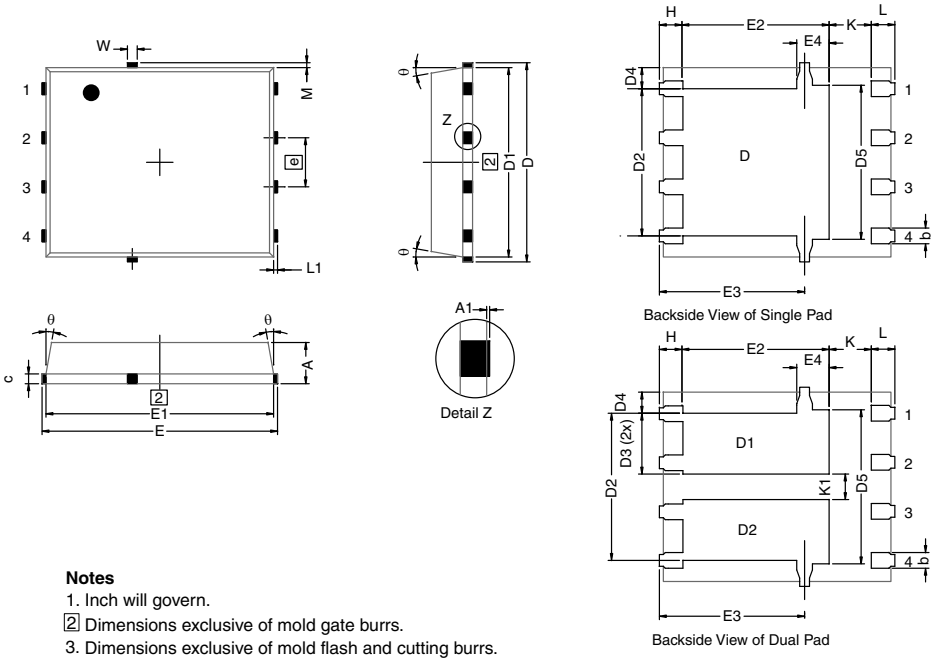


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

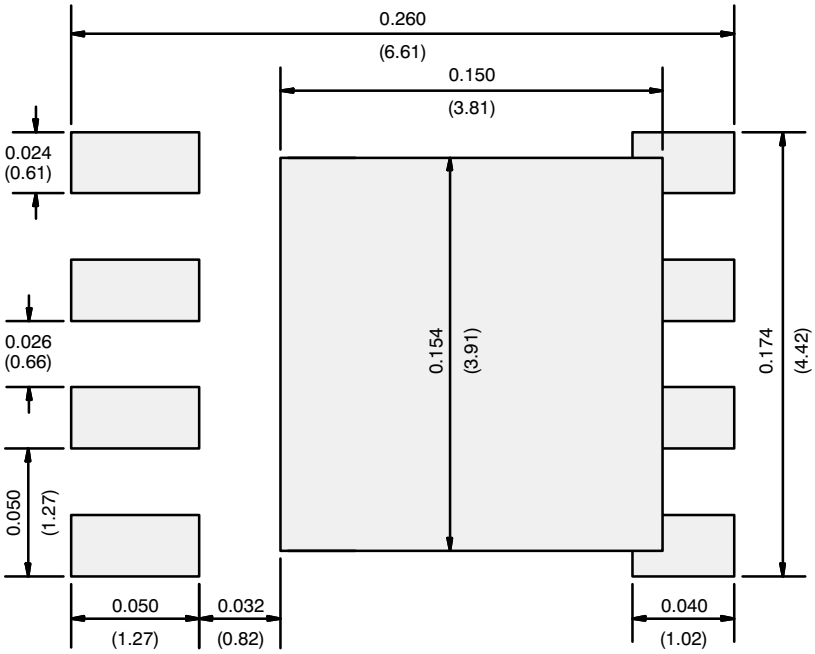
PowerPAK® SO-8, (Single/Dual)



Notes
1. Inch will govern.
2 Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4		0.57 typ.			0.0225 typ.	
D5		3.98 typ.			0.157 typ.	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4		0.75 typ.			0.030 typ.	
e		1.27 BSC			0.050 BSC	
K		1.27 typ.			0.050 typ.	
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M		0.125 typ.			0.005 typ.	
ECN: S17-0173-Rev. L, 13-Feb-17 DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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