

P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-60
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.0060
$R_{DS(on)}$ (Ω) at $V_{GS} = -4.5$ V	0.0075
I_D (A)	-80
Configuration	Single
Package	DFN 5X6

FEATURES

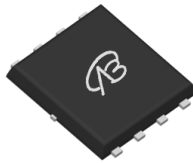
- Trench power MOSFET
- 100 % R_g and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE

DFN5X6

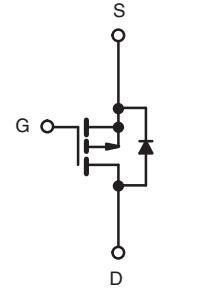
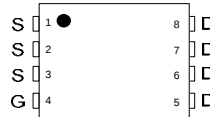
Top View



Bottom View



Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	I_D	-80	A
		-64	
Continuous Source Current (Diode Conduction) ^a	I_S	-80	
Pulsed Drain Current ^b	I_{DM}	-240	
Single Pulse Avalanche Current	I_{AS}	-36	mJ
Single Pulse Avalanche Energy	E_{AS}	64.8	
Maximum Power Dissipation ^b	P_D	68	W
		22	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	68	$^\circ\text{C/W}$
Junction-to-Case (Drain)	R_{thJC}	2.2	

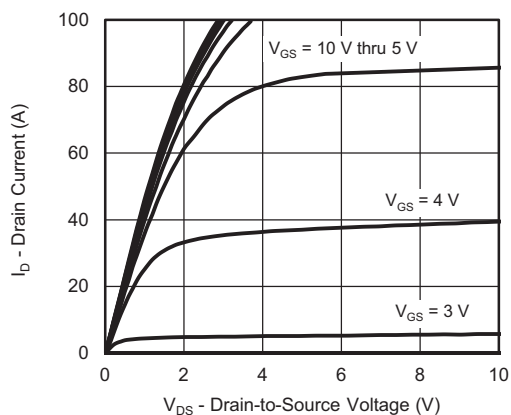
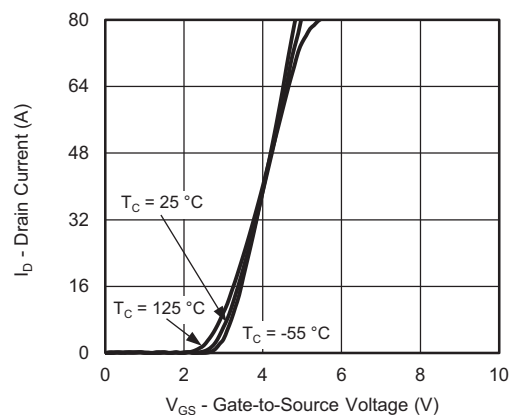
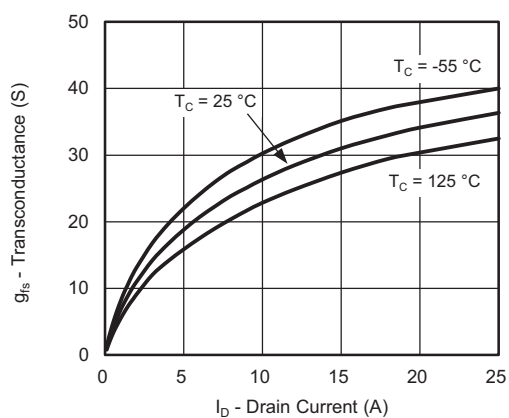
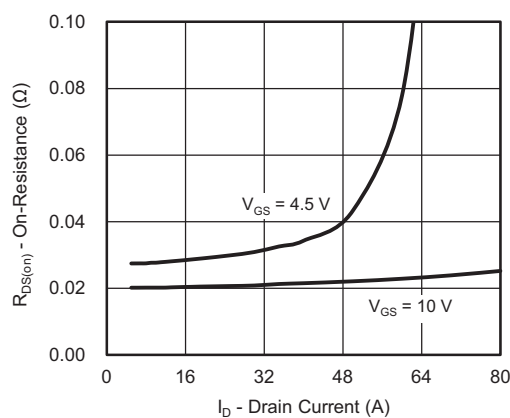
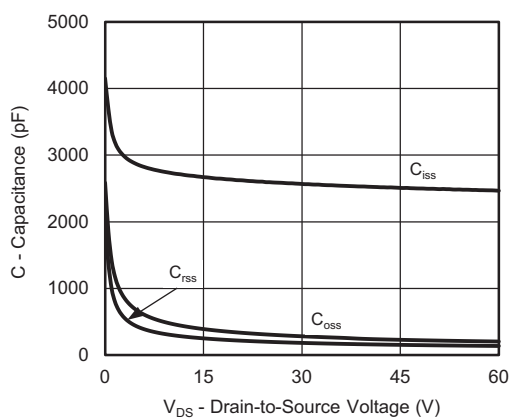
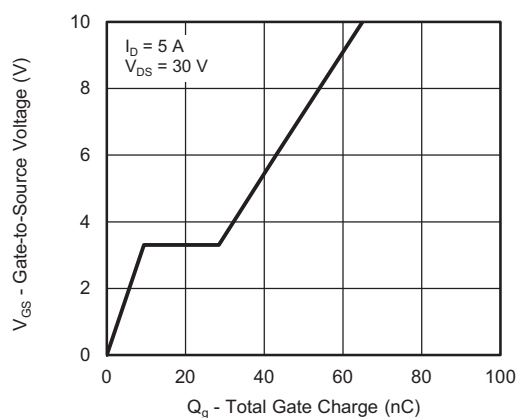
Notes

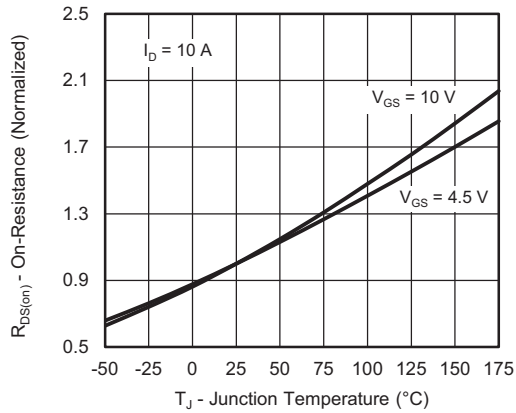
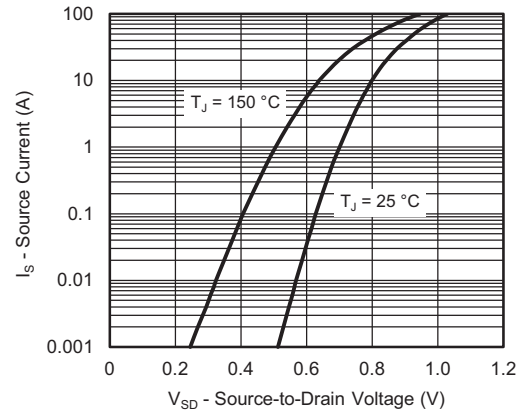
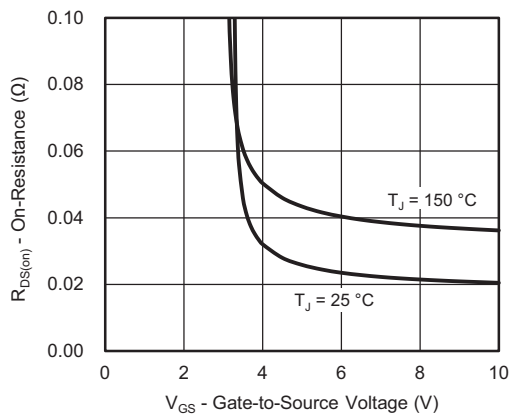
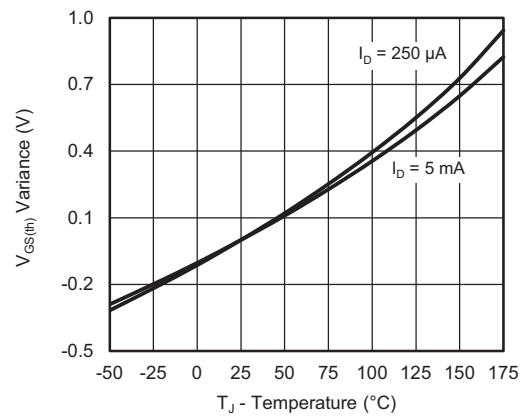
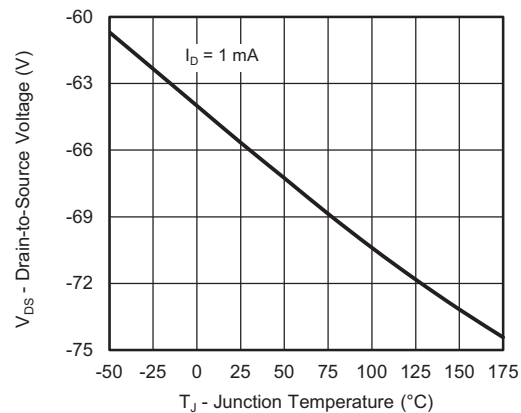
- Package limited.
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR4 material).

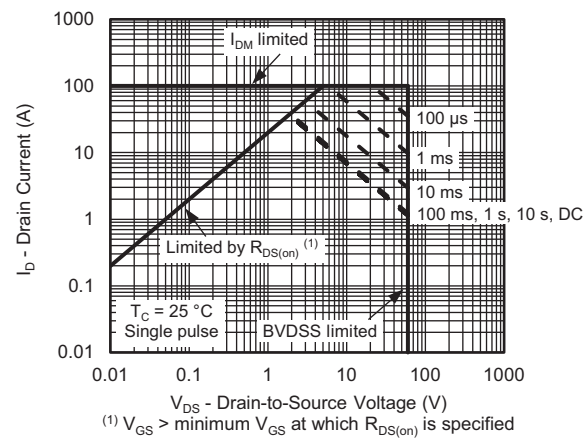
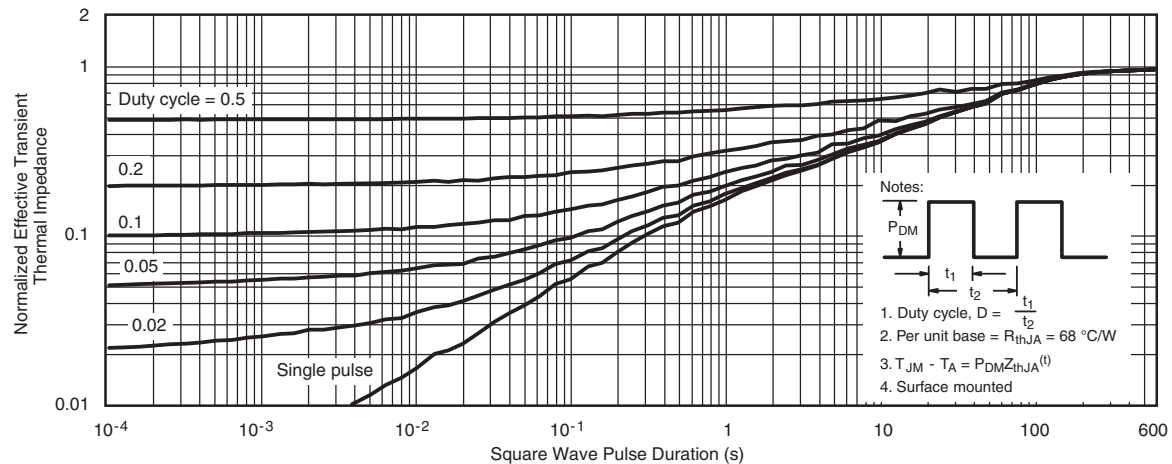
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = -250 μA		-60	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA		-	3	-	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = -60 V	-	-	-1	μA
		V _{GS} = 0 V	V _{DS} = -48 V, T _J = 125 °C	-	-	-50	
		V _{GS} = 0 V	V _{DS} = -48 V, T _J = 175 °C	-	-	-150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = -10 V	V _{DS} ≥ -5 V	-30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V	I _D = -10 A	-	0.0060	-	Ω
		V _{GS} = -10 V	I _D = -10 A, T _J = 125 °C	-	0.0120	-	
		V _{GS} = -10 V	I _D = -10 A, T _J = 175 °C	-	0.0150	-	
		V _{GS} = -4.5 V	I _D = -10 A	-	0.0075	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -10 A		-	26	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	-	12000		pF
Output Capacitance	C _{oss}			-	310	450	
Reverse Transfer Capacitance	C _{rss}			-	200	275	
Total Gate Charge ^c	Q _g	V _{GS} = -10 V	V _{DS} = -30 V, I _D = -5 A	-	6.0	100	nC
Gate-Source Charge ^c	Q _{gs}			-	9.5	-	
Gate-Drain Charge ^c	Q _{gd}			-	19	-	
Gate Resistance	R _g	f = 1 MHz		0.50	1.19	1.80	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = -30 V, R _L = 6 Ω I _D ≅ -5 A, V _{GEN} = -10 V, R _g = 1 Ω		-	15	25	ns
Rise Time ^c	t _r			-	5	10	
Turn-Off Delay Time ^c	t _{d(off)}			-	40	75	
Fall Time ^c	t _f			-	6	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	- 240	A
Forward Voltage	V _{SD}	I _F = -10 A, V _{GS} = 0 V		-	-0.80	-1.2	V

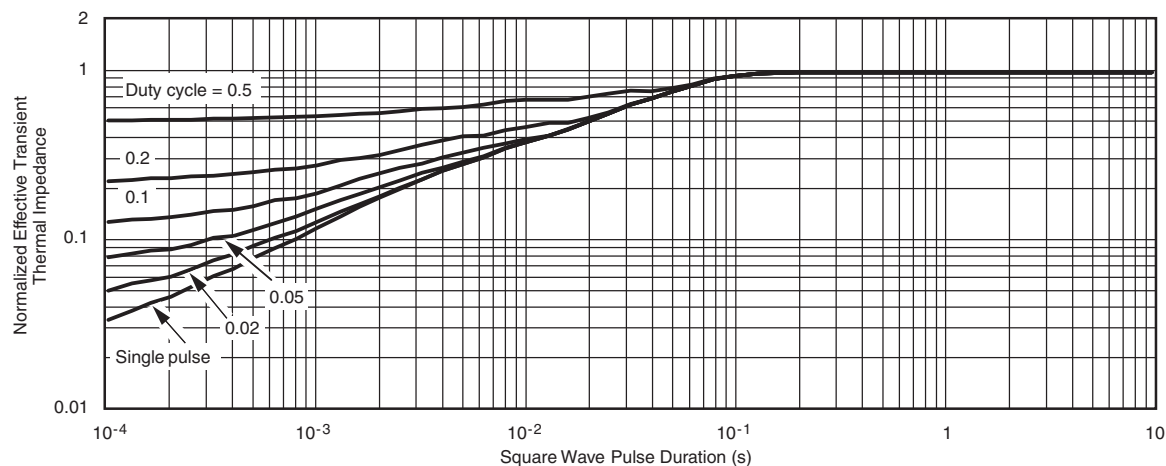
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

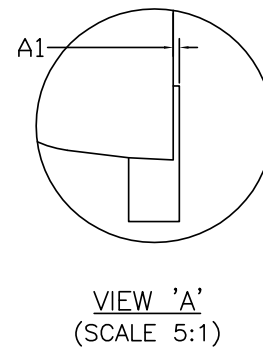
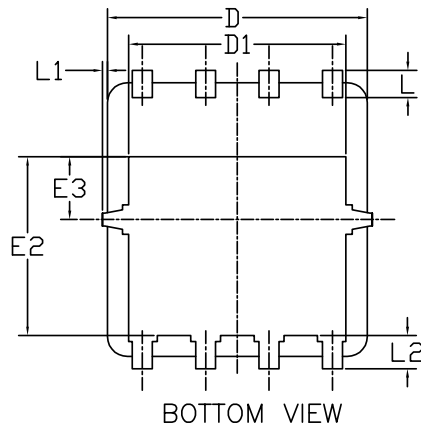
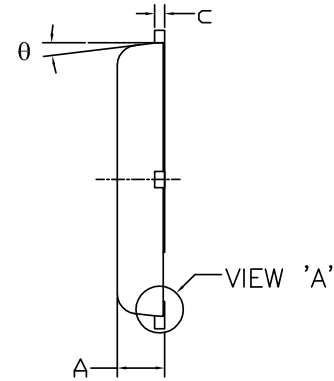
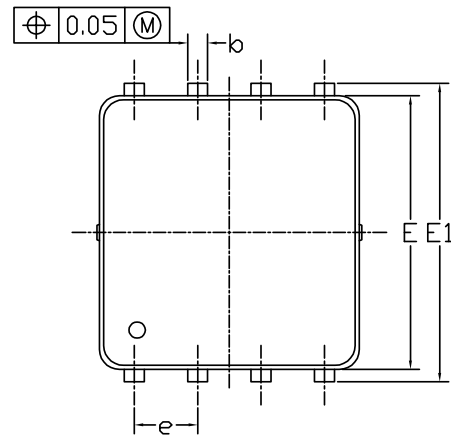
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain-Source Breakdown vs. Junction Temperature

THERMAL RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

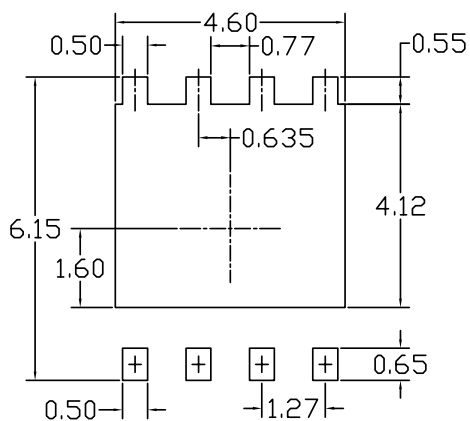
THERMAL RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

NOTE

- PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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