

N-Channel 650V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.42
Q_g max. (nC)	38	
Q_{gs} (nC)	4	
Q_{gd} (nC)	4.2	
Configuration	Single	

FEATURES

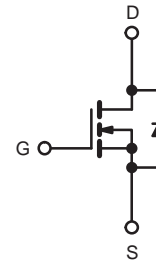
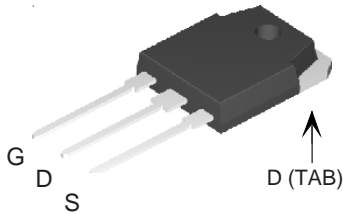
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

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
N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	11
		$T_C = 100$ °C	9.7
Pulsed Drain Current ^a		I_{DM}	55
Linear Derating Factor			1.67/1.5/0.3
Single Pulse Avalanche Energy ^b		E_{AS}	132
Maximum Power Dissipation		P_D	83/83/31
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150
Drain-Source Voltage Slope		dV/dt	50
Reverse Diode dV/dt ^d	$T_J = 125$ °C		3.1
Soldering Recommendations (Peak Temperature) ^c	for 10 s		300
			°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	60	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.6	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.65	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}$	-	0.42	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 5\text{ A}$		-	16	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$		-	680	-	pF
Output Capacitance	C_{oss}			-	140	-	
Reverse Transfer Capacitance	C_{rss}			-	5	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$		-	63	-	pF
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	113	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 5\text{ A}, V_{DS} = 520\text{ V}$	-	38	56	nC
Gate-Source Charge	Q_{gs}			-	4	-	
Gate-Drain Charge	Q_{gd}			-	4.5	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 5\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	13	25	ns
Rise Time	t_r			-	11	35	
Turn-Off Delay Time	$t_{d(off)}$			-	81	90	
Fall Time	t_f			-	25	40	
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		-	3.5	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	11	A
Pulsed Diode Forward Current	I_{SM}			-	-	55	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 5\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$		-	270	-	ns
Reverse Recovery Charge	Q_{rr}			-	3.3	-	μC
Reverse Recovery Current	I_{RRM}			-	30	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics

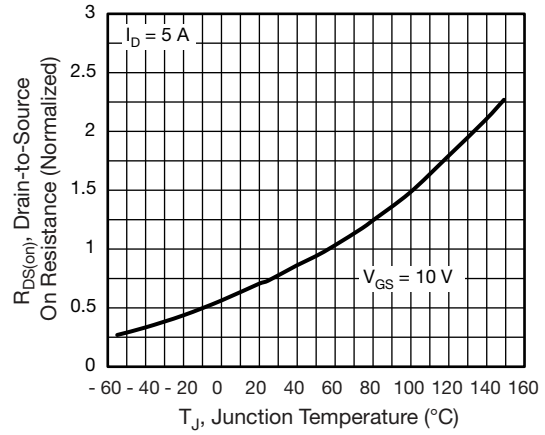


Fig. 4 - Normalized On-Resistance vs. Temperature

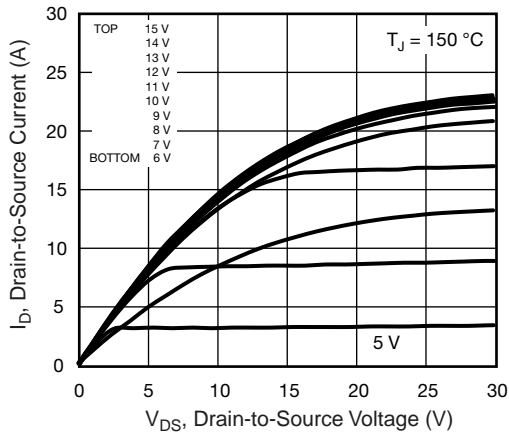


Fig. 2 - Typical Output Characteristics

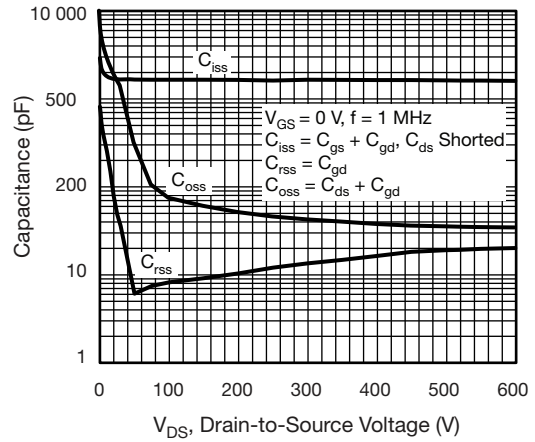


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

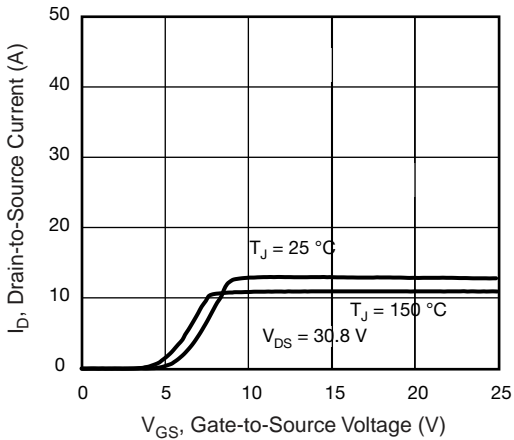


Fig. 3 - Typical Transfer Characteristics



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

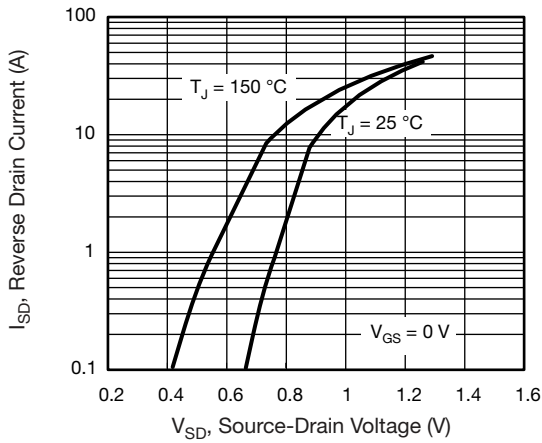


Fig. 7 - Typical Source-Drain Diode Forward Voltage

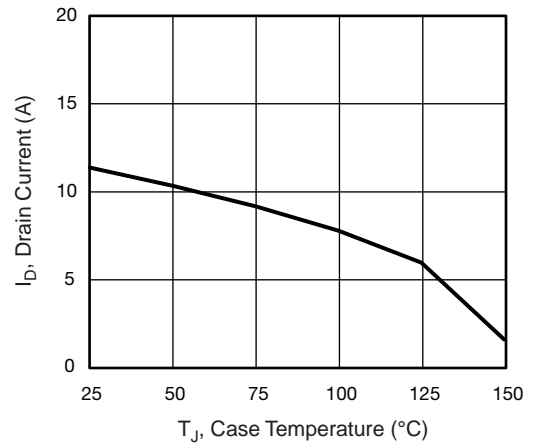


Fig. 9 - Maximum Drain Current vs. Case Temperature

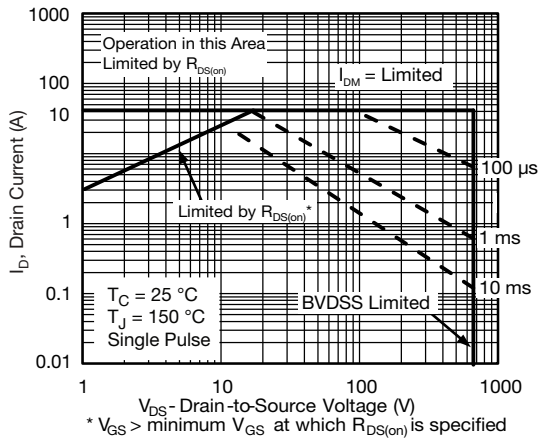


Fig. 8 - Maximum Safe Operating Area

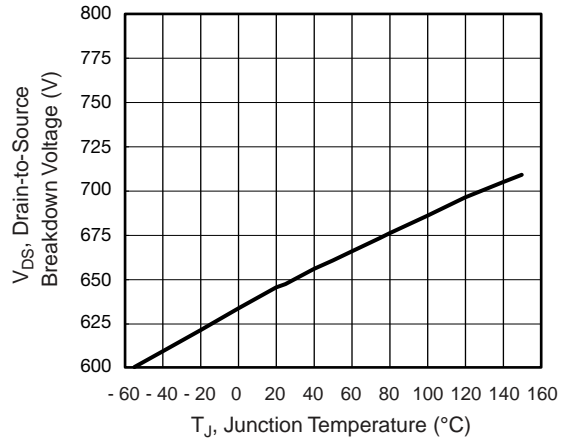


Fig. 10 - Temperature vs. Drain-to-Source Voltage



Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

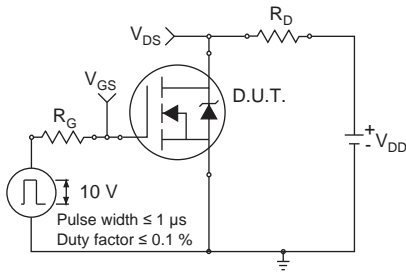


Fig. 12 - Switching Time Test Circuit

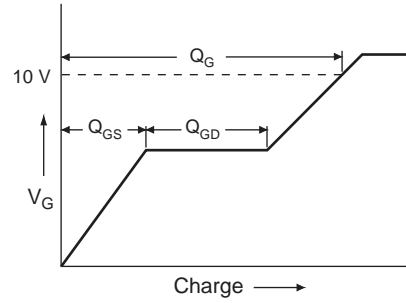


Fig. 16 - Basic Gate Charge Waveform

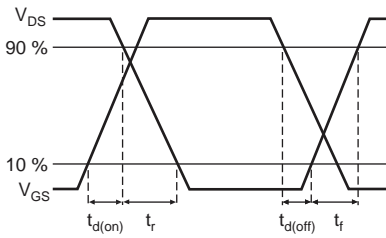


Fig. 13 - Switching Time Waveforms

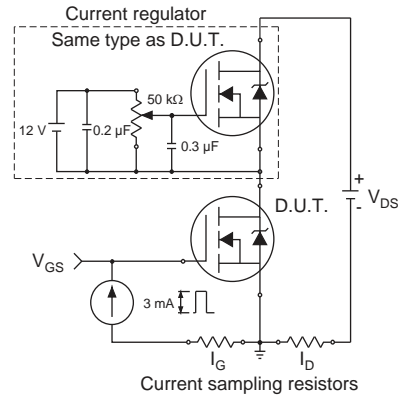


Fig. 17 - Gate Charge Test Circuit

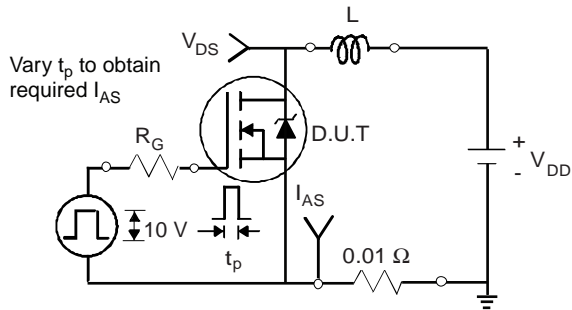


Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms

Peak Diode Recovery dV/dt Test Circuit

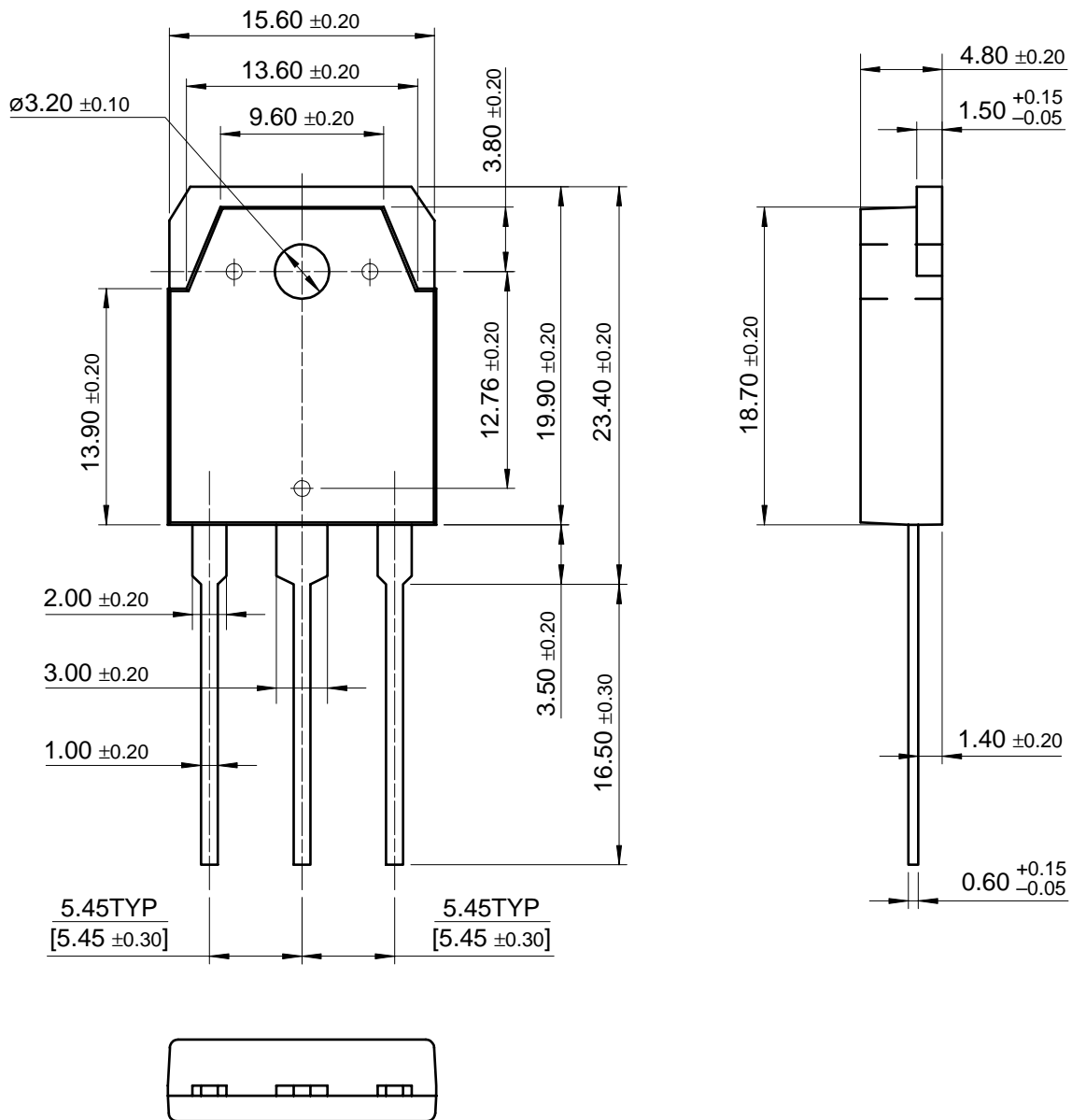


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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