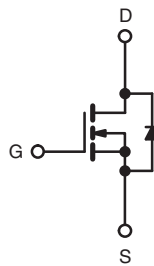
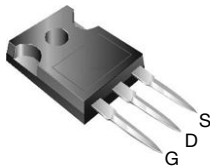


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	650
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$   0.24
$Q_g$ (Max.) (nC)	150
$Q_{gs}$ (nC)	45
$Q_{gd}$ (nC)	76
Configuration	Single

TO-247AC



N-Channel MOSFET

### FEATURES

- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode  $dV/dt$  Capability
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT

### BENEFITS

- Hard Switching Primary or PFS Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

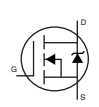
ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	22
		$T_C = 100\text{ }^\circ\text{C}$	14
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	88	A
Linear Derating Factor		2.9	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	380	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	22	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	37	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	370
Peak Diode Recovery $dV/dt^c$		$dV/dt$	15
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1.5\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 22\text{ A}$  (see fig. 12).
- $I_{SD} \leq 22\text{ A}$ ,  $dI/dt \leq 360\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.34	

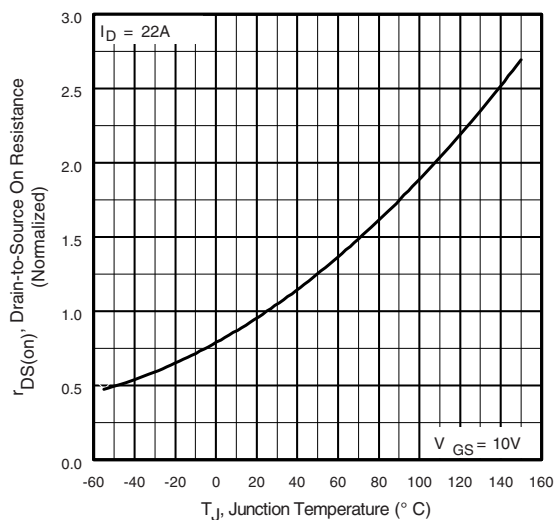
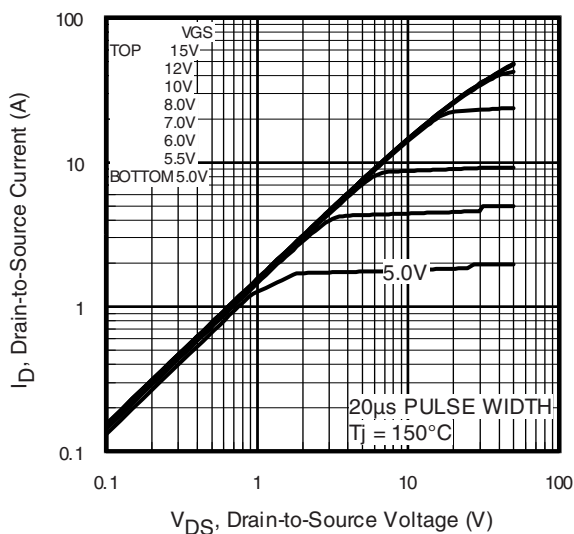
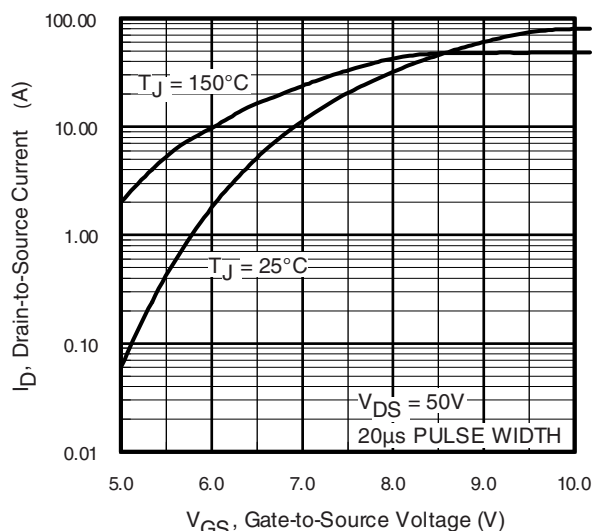
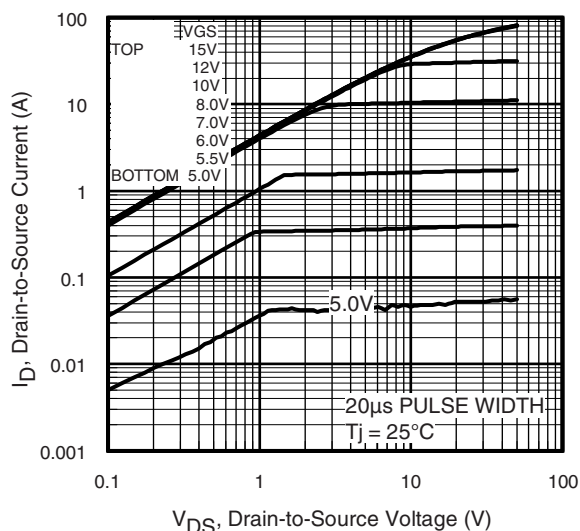
**SPECIFICATIONS** ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$	-	0.30	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}^b$	-	0.240	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 13\text{ A}^b$	11	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	3570	-	pF
Output Capacitance	$C_{oss}$		-	350	-	
Reverse Transfer Capacitance	$C_{rss}$		-	36	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	4710	-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	92	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	180	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 22\text{ A}, V_{DS} = 480\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	150	nC
Gate-Source Charge	$Q_{gs}$		-	-	45	
Gate-Drain Charge	$Q_{gd}$		-	-	76	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 22\text{ A}, R_g = 6.2, V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b</sup>	-	26	-	ns
Rise Time	$t_r$		-	99	-	
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	
Fall Time	$t_f$		-	37	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	22	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	88	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 22\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$	-	590	890	ns
		$T_J = 125\text{ }^\circ\text{C}$	-	670	1010	
Body Diode Reverse Recovery Charge	$Q_{rr}$	$T_J = 25\text{ }^\circ\text{C}$	-	7.2	11	$\mu\text{C}$
		$T_J = 125\text{ }^\circ\text{C}$	-	8.5	13	
Reverse Recovery Current	$I_{RRM}$	$T_J = 25\text{ }^\circ\text{C}$	-	26	39	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



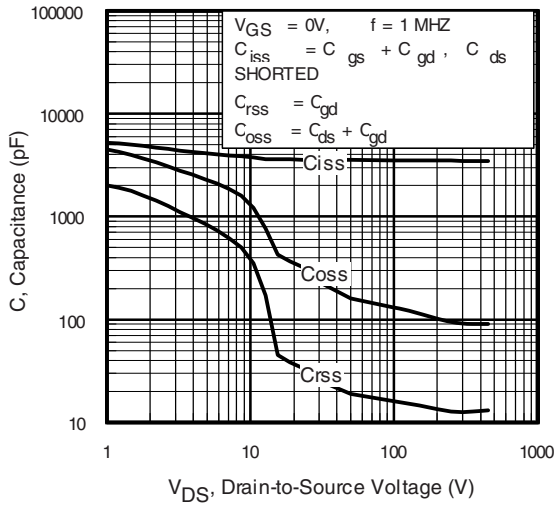


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

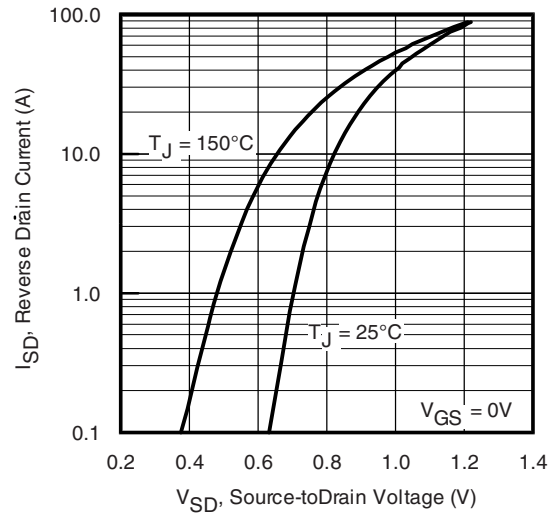


Fig. 7 - Typical Source-Drain Diode Forward Voltage

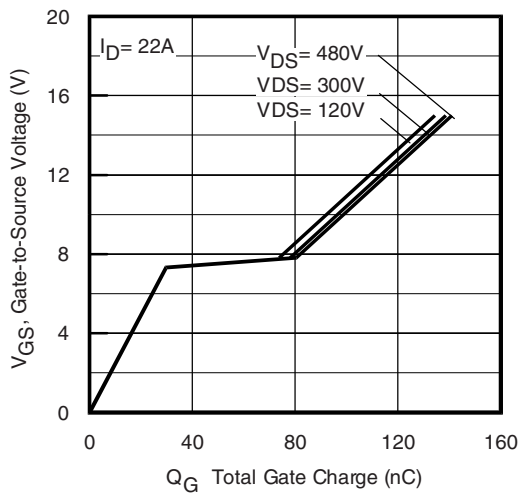


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

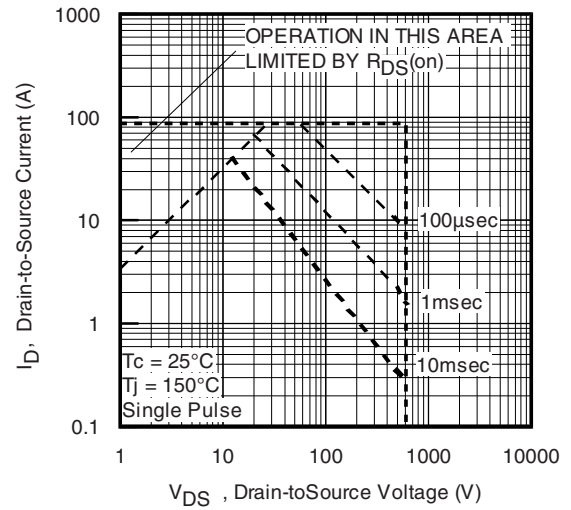


Fig. 8 - Maximum Safe Operating Area

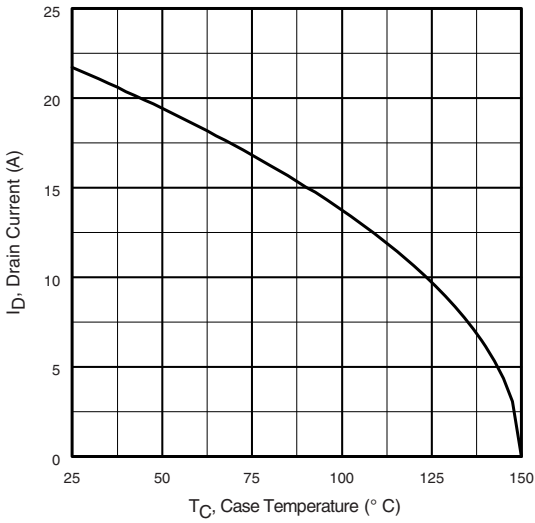


Fig. 9 - Maximum Drain Current vs. Case Temperature

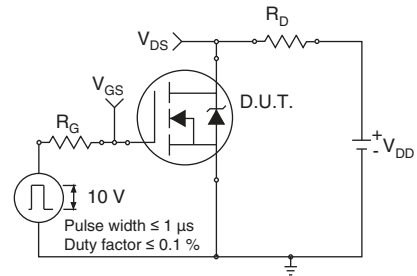


Fig. 10a - Switching Time Test Circuit

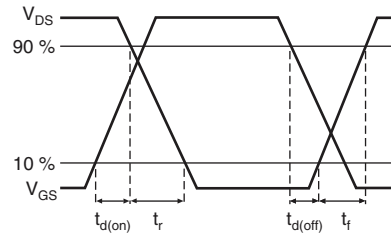


Fig. 10b - Switching Time Waveforms

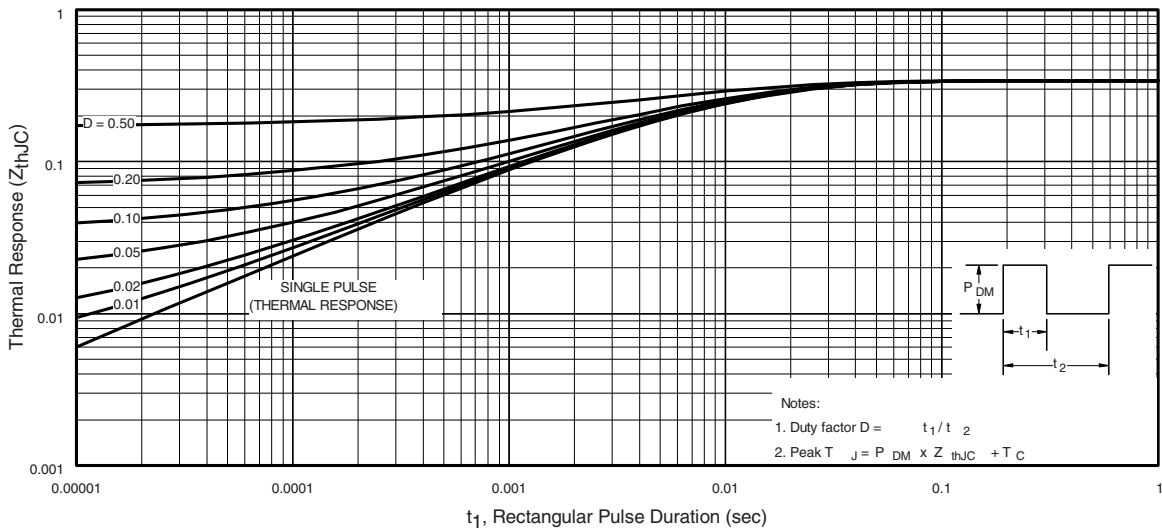


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

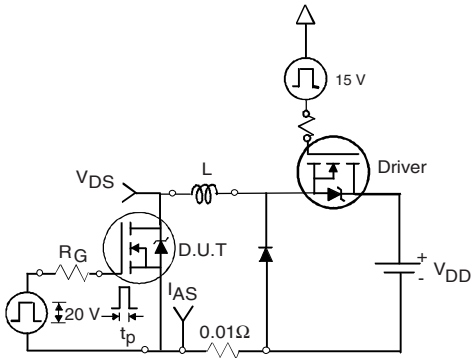


Fig. 12a - Unclamped Inductive Test Circuit

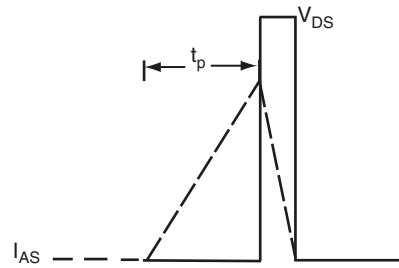


Fig. 12b - Unclamped Inductive Waveforms

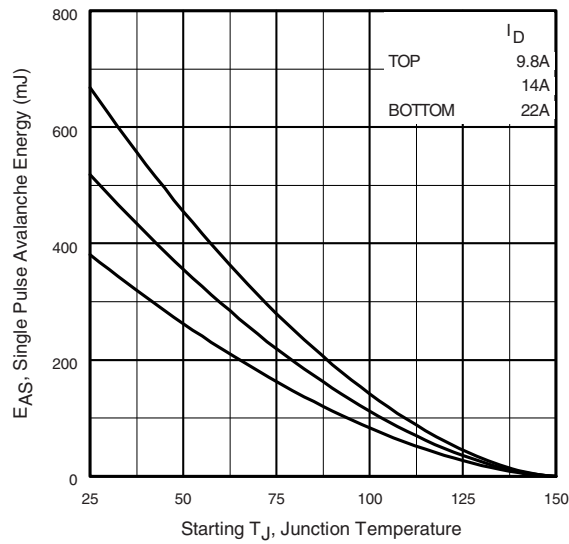


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

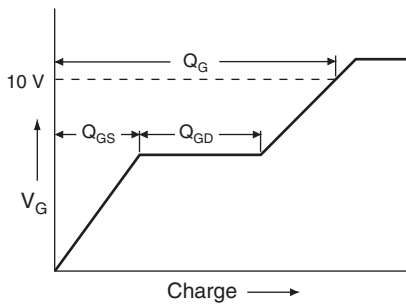


Fig. 13a - Basic Gate Charge Waveform

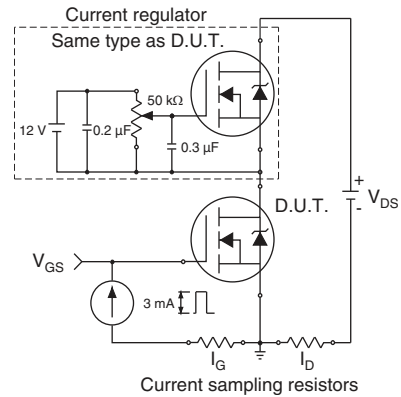
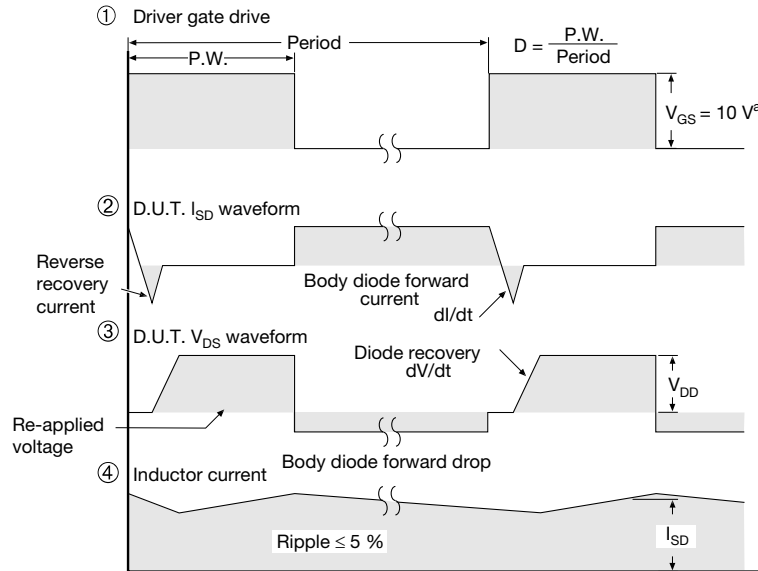
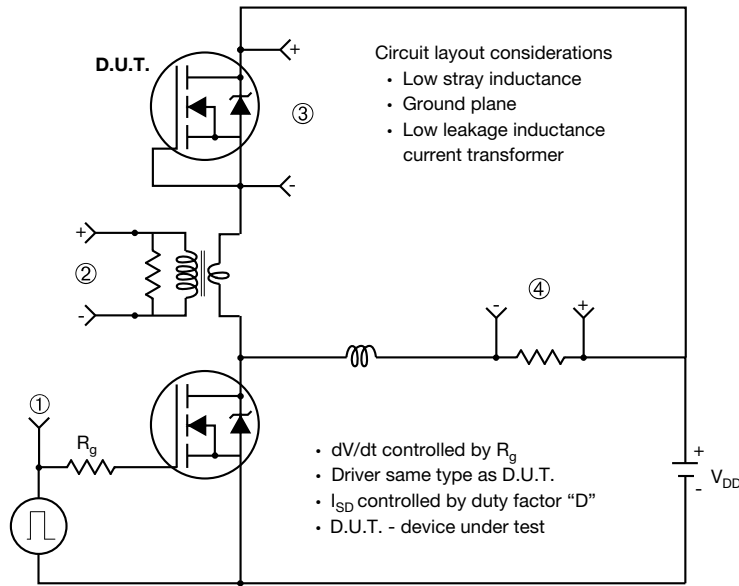


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

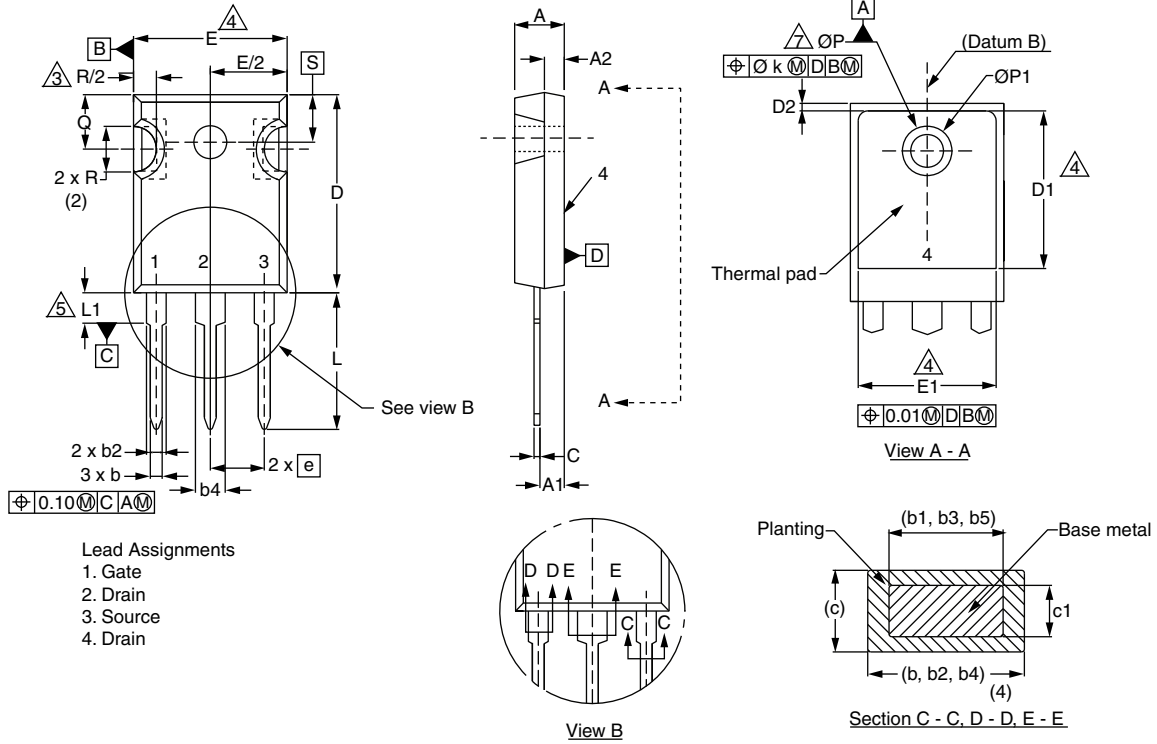


**Note**

a.  $V_{GS} = 5V$  for logic level devices

**Fig. 14 - For N-Channel**

# TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
$\phi k$	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
$\phi P$	3.51	3.66	0.138	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13  
 DWG: 5971



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