

# N-Channel 60-V (D-S) Super Trench Power MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	60				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0049				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0055				
I <sub>D</sub> (A)	97				
Configuration	Single				

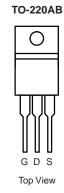
### **FEATURES**

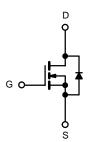
- Super Trench technology Power MOSFET
- Excellent gate charge x Rds (on) product(FOM)
- Very low on-resfistance Rds (on)
- 100 % R<sub>g</sub> and UIS Tested



## **APPLICATIONS**

• Isolated DC/DC Converters





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	60	V	
Gate-Source Voltage		$V_{GS}$	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C	1	97		
	T <sub>C</sub> = 125 °C	- I <sub>D</sub>	56		
Continuous Source Current (Diode Conduction) <sup>a</sup>		Is	100	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	360		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	45		
Single Pulse Avalanche Energy		E <sub>AS</sub>	101	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	136	W	
	T <sub>C</sub> = 125 °C	FD	45	VV	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W		
Junction-to-Case (Drain)		$R_{thJC}$	0.4	C/ VV		

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	1			·				
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60	-	-	.,	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 \text{ V}$	50	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 25 A	-	0.0049	-	Ω	
Dunin Course On Otata Basistanas		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 25 A, T <sub>J</sub> = 125 °C	-	0.0117	-		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 25 A, T <sub>J</sub> = 175 °C	-	0.0149	-		
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	-	0.0055	-		
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		-	177	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 V V <sub>DS</sub> = 25 V, f = 1 MHz	-	4844	6060	pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	441	555		
Reverse Transfer Capacitance	C <sub>rss</sub>	1		-	200	250		
Total Gate Charge <sup>c</sup>	Qg			-	82	125		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, I_{D} = 50 \text{ A}$	-	14.5	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	1		-	13.5	-		
Gate Resistance	$R_g$	f = 1 MHz		1	2	3	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 30 \text{ V}, \text{ R}_{L} = 0.6 \Omega$ $I_{D} \cong 50 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	14	21		
Rise Time <sup>c</sup>	t <sub>r</sub>			-	5	8	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	41	62		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	7	11		
Source-Drain Diode Ratings and Char-	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	290	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		-	0.9	1.5	V	

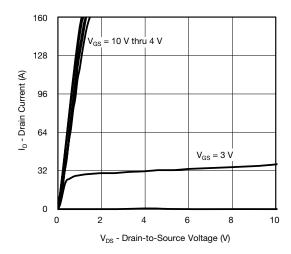
## Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

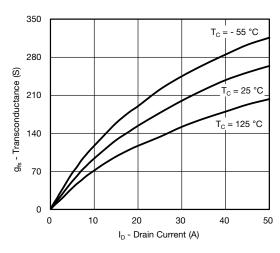
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



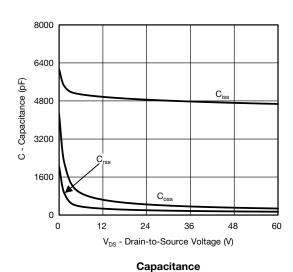
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

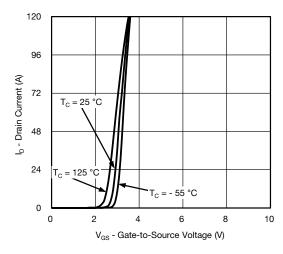


## **Output Characteristics**

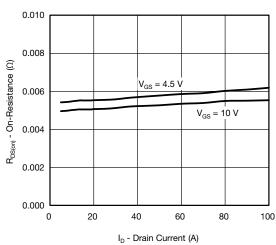


## Transconductance

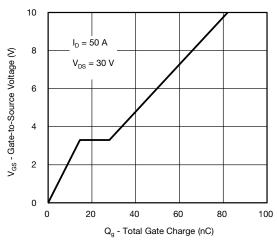




#### **Transfer Characteristics**



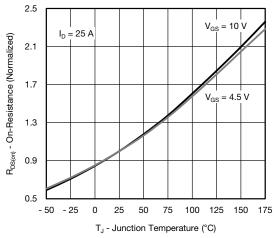
### On-Resistance vs. Drain Current



**Gate Charge** 



# TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



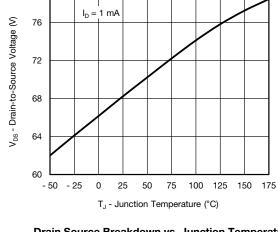
**On-Resistance vs. Junction Temperature Drain Source Breakdown vs. Junction Temperature** 

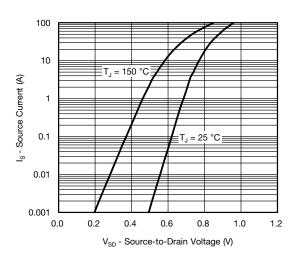
0.05

0.04

0.03

80

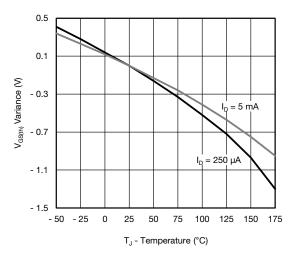




R<sub>DS(on)</sub> - On-Resistance (Ω) 0.02  $T_J = 150 \, ^{\circ}C$ 0.01  $T_J = 25 \, ^{\circ}C$ 0.00 4 6 10

**Source Drain Diode Forward Voltage** 

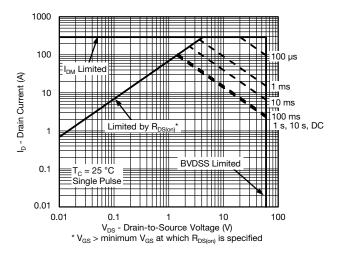
V<sub>GS</sub> - Gate-to-Source Voltage (V) On-Resistance vs. Gate-to-Source Voltage



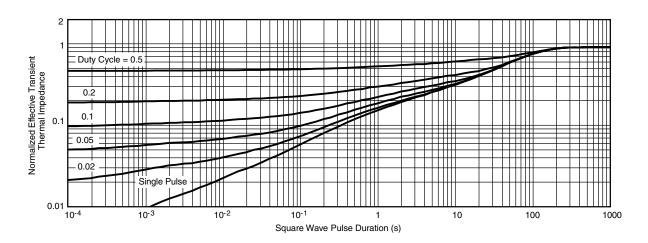
**Threshold Voltage** 



# **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



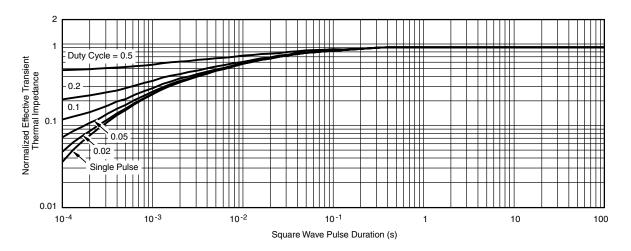
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

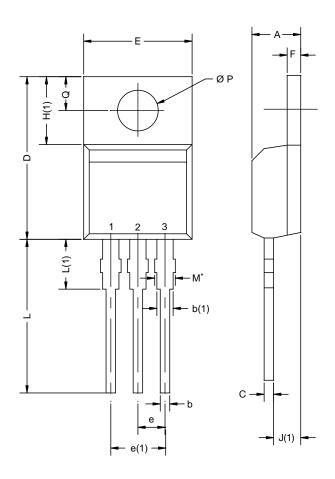
#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



# **TO-220AB**



	MILLIM	IETERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471					

## Notes

 $^{\star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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