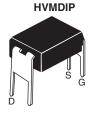


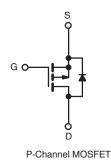
Power MOSFET

PRODUCT SUMMA	RY		
V _{DS} (V)	- 10	0	
R _{DS(on)} (Ω)	V _{GS} = - 10 V	1.0	
Q _g (Max.) (nC)	8.7		
Q _{gs} (nC)	2.2		
Q _{gd} (nC)	4.1		
Configuration	Sing	le	

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- 175 °C Operating Temperature
- · Fast Switching
- Compliant to RoHS Directive 2002/95/EC





PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	- 100	V	
Gate-Source Voltage		V _{GS}	± 20	- V	
Continuous Drain Current	$V_{GS} \text{ at } -10 \text{ V} \frac{T_A = 25 \text{ °C}}{T_A = 100 \text{ °C}}$	I _D	- 0.70	A	
Continuous Drain Current	$T_{A} = 100 ^{\circ}\text{C}$		- 0.49		
Pulsed Drain Current ^a		I _{DM}	- 5.6		
Linear Derating Factor			0.0083	W/°C	
Single Pulse Avalanche Energy ^b		E _{AS}	140	mJ	
Repetitive Avalanche Current ^a		I _{AR}	- 0.7	А	
Repetitive Avalanche Energy ^a		E _{AR}	0.13	mJ	
Maximum Power Dissipation	T _A = 25 °C	P _D	1.3	W	
Peak Diode Recovery dV/dt ^c		dV/dt	- 5.5	V/ns	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175		
Soldering Recommendations (Peak Temperature)	for 10 s	-	300 ^d		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD} = -25 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 52 mH, $R_g = 25 \Omega$, $I_{AS} = -2.0 \text{ A}$ (see fig. 12). c. $I_{SD} \le -4.0 \text{ A}$, dI/dt $\le 75 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \text{ °C}$. d. 1.6 mm from case.

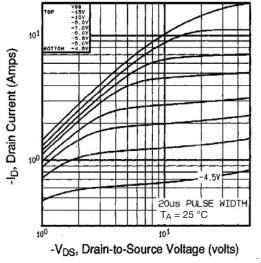


THERMAL RESISTANCE RATI	NGS							
PARAMETER	SYMBOL	TYP.		MAX. 120			UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-				°C/W		
SPECIFICATIONS ($T_J = 25 \text{ °C}$, u	nless otherw	ise noted)						-
PARAMETER	SYMBOL	TES	T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT
Static								-
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	= 0 V, I _D = -	· 250 µA	- 100	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C,	I _D = - 1 mA	-	- 0.091	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$		- 2.0	-	- 4.0	V	
Gate-Source Leakage	I _{GSS}	$V_{GS} = \pm 20 V$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =	- 100 V, V	_{GS} = 0 V	-	-	- 100	μA
Zero date voltage Brain ourient	$V_{DS} = -80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 150 \text{ °C}$		V, T _J = 150 °C	-	-	- 500	μΛ	
Drain-Source On-State Resistance	R _{DS(on)}	$V_{GS} = -10 V$	I _D :	= - 0.42 A ^b	-	1.0	-	Ω
Forward Transconductance	9 _{fs}	V _{DS} =	- 50 V, I _D =	- 0.42 A	0.60	-	-	S
Dynamic								
Input Capacitance	C _{iss}	$V_{GS} = 0 V,$		-	200	-		
Output Capacitance	C _{oss}		V _{DS} = - 25	V,	-	94	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1	.0 MHz, se	e fig. 5	-	18	-	
Total Gate Charge	Qg			0 A, V _{DS} = - 80 V	-	-	8.7	
Gate-Source Charge	Q _{gs}	V_{GS} = - 10 V		ig. 6 and 13^{b}	-	-	2.2	nC
Gate-Drain Charge	Q _{gd}		5001	ig. o una ro	-	-	4.1	
Turn-On Delay Time	t _{d(on)}	N -	50 V I	- 40 4	-	10	-	
Rise Time	t _r	V_{DD} = - 50 V, I _D = - 4.0 A R_g = 24 Ω , R_D = 11 Ω , see fig. 10 ^b		-	27	-	- ns	
Turn-Off Delay Time	t _{d(off)}			-	15	-		
Fall Time	t _f			-	17	-		
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH	
Internal Source Inductance	L _S			-	6.0	-		
Drain-Source Body Diode Characteristic	s							
Continuous Source-Drain Diode Current	I _S	MOSFET sym showing the			-	-	- 0.70	A
Pulsed Diode Forward Current ^a	I _{SM}	integral revers p - n junction			-	-	- 5.6	~
Body Diode Voltage	V_{SD}	T _J = 25 °C	, I _S = - 0.7	A, V _{GS} = 0 V ^b	-	-	- 5.5	V
Body Diode Reverse Recovery Time	t _{rr}	T 25 °C I	- 404 -	dl/dt = 100 A/µs ^b	-	82	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$J = 25 \text{ C}, I_{\text{F}}$	= - 4.0 A, C	$\mu/\alpha t = 100 A/\mu S^{3}$	-	0.15	0.30	μC

Notes

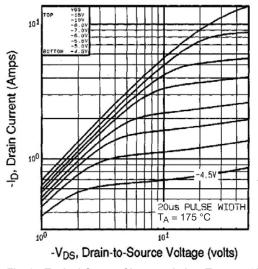
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width \leq 300 µs; duty cycle \leq 2 %.





TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)







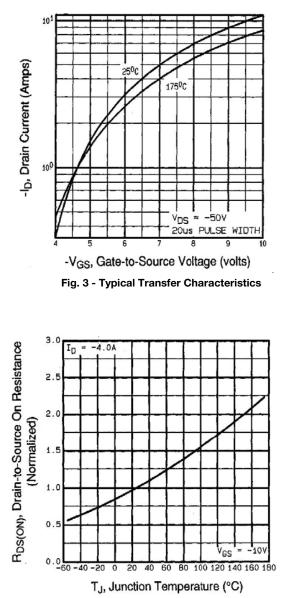


Fig. 4 - Normalized On-Resistance vs. Temperature

VBGC2101K



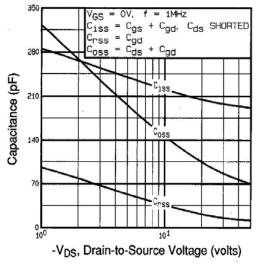
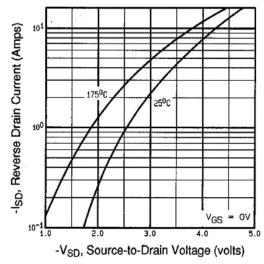


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage





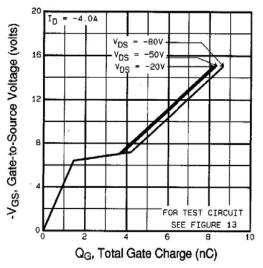
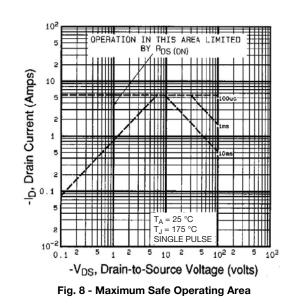


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage





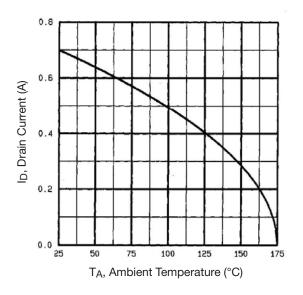


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

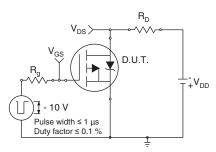


Fig. 10a - Switching Time Test Circuit

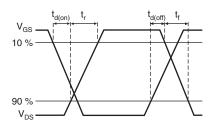


Fig. 10b - Switching Time Waveforms

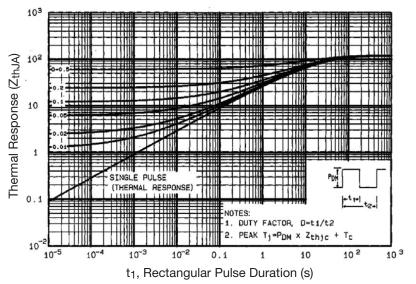


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



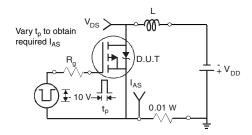


Fig. 12a - Unclamped Inductive Test Circuit

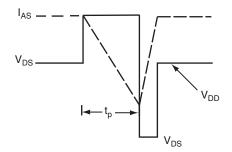


Fig. 12b - Unclamped Inductive Waveforms

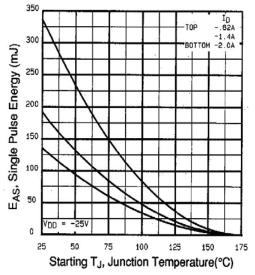


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

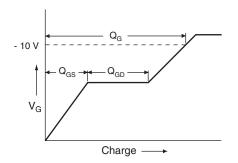


Fig. 13a - Basic Gate Charge Waveform

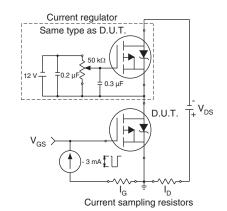
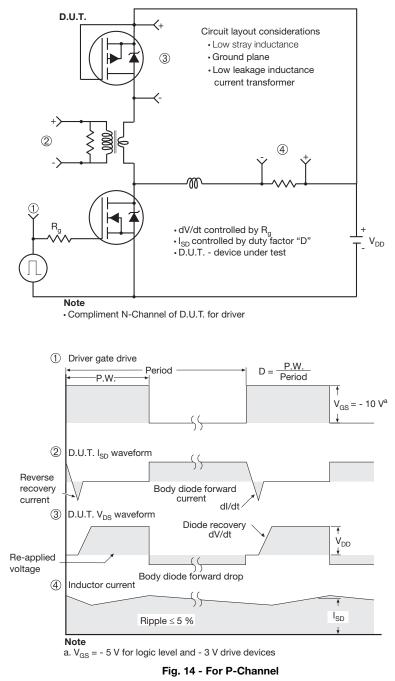


Fig. 13b - Gate Charge Test Circuit

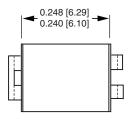


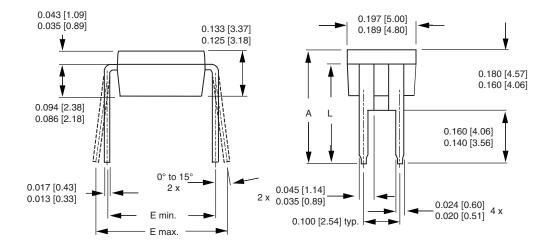
Peak Diode Recovery dV/dt Test Circuit





HVM DIP (High voltage)





DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
А	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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