

## P-Channel 500 V (D-S) Power MOSFET

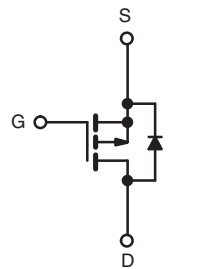
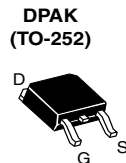
PRODUCT SUMMARY		
$V_{DS}$ (V)	- 500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	2.0
$Q_g$ (Max.) (nC)	13	
$Q_{gs}$ (nC)	3.2	
$Q_{gd}$ (nC)	5.0	
Configuration	Single	

### FEATURES

- P-Channel
- Surface Mount (IRFR9310, SiHFR9310)
- Straight Lead (IRFU9310, SiHFU9310)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	- 500	V	
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at - 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	- 4.0	A
			$T_C = 100\text{ }^\circ\text{C}$	- 3.1	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	-15		
Linear Derating Factor			0.40	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	92	mJ	
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	- 4	A	
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	15.0	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	80	W	
Peak Diode Recovery $dV/dt^c$		$dV/dt$	- 24	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300		


### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 57\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = - 1.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq - 1.1\text{ A}$ ,  $dI/dt \leq 450\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	2.5	

**Note**

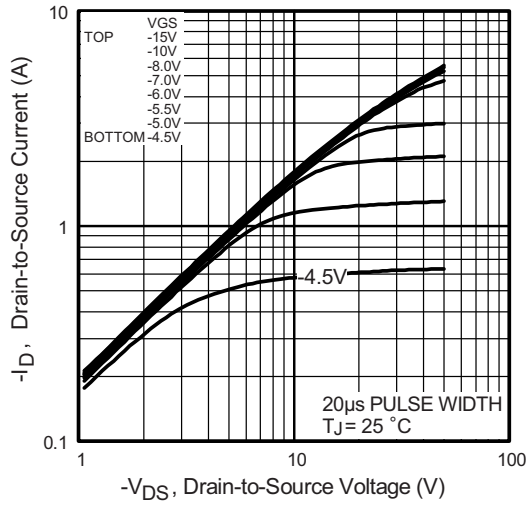
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		- 500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	- 0.41	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$		-	-	- 100	$\mu\text{A}$
		$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -3.1\text{ A}^b$	-	2	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -3.1\text{ A}$		0.91	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	270	-	pF
Output Capacitance	$C_{oss}$			-	50	-	
Reverse Transfer Capacitance	$C_{rss}$			-	8.0	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -1.1\text{ A}, V_{DS} = -320\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	13	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.2	
Gate-Drain Charge	$Q_{gd}$			-	-	5.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -200\text{ V}, I_D = -1.1\text{ A}, R_g = 21\text{ }\Omega, R_D = 180\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	10	-	
Turn-Off Delay Time	$t_{d(off)}$			-	25	-	
Fall Time	$t_f$			-	24	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact <sup>c</sup>		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.9	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	- 7.6	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	- 4.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	170	260	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	640	960	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

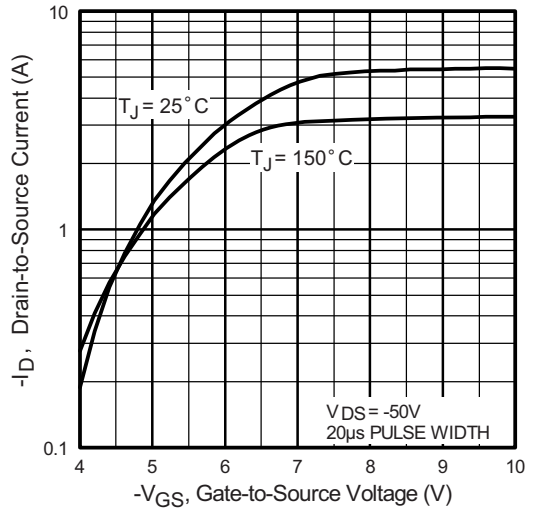
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c. This is applied for IPAK,  $L_S$  of DPAK is measured between lead and center of die contact.

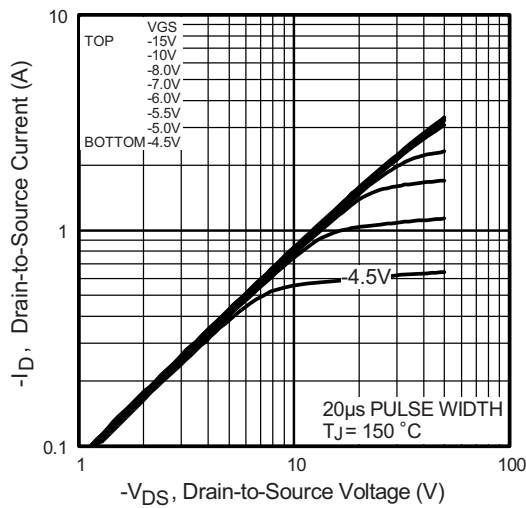
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



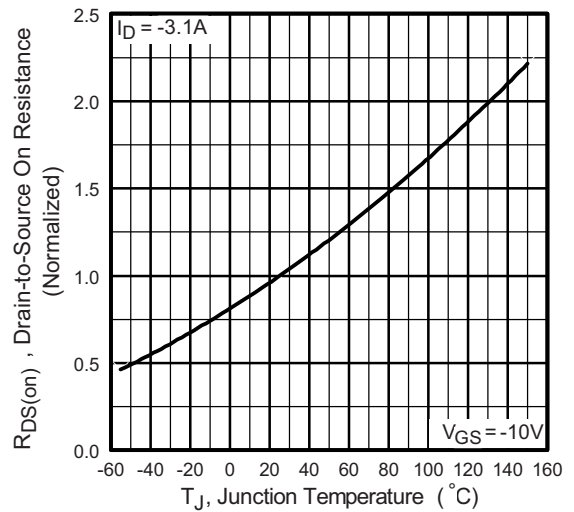
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

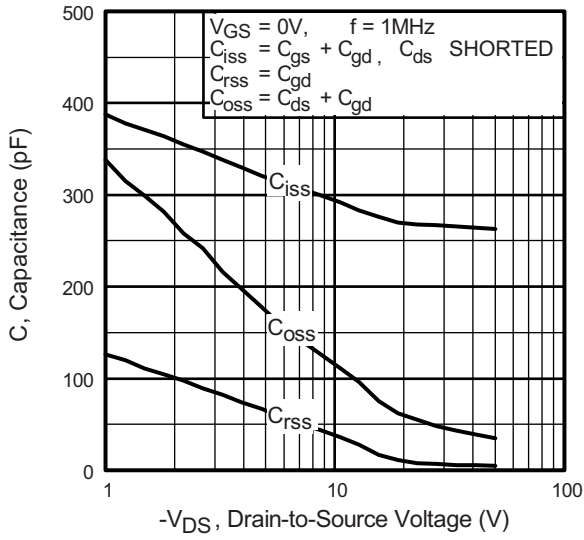


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

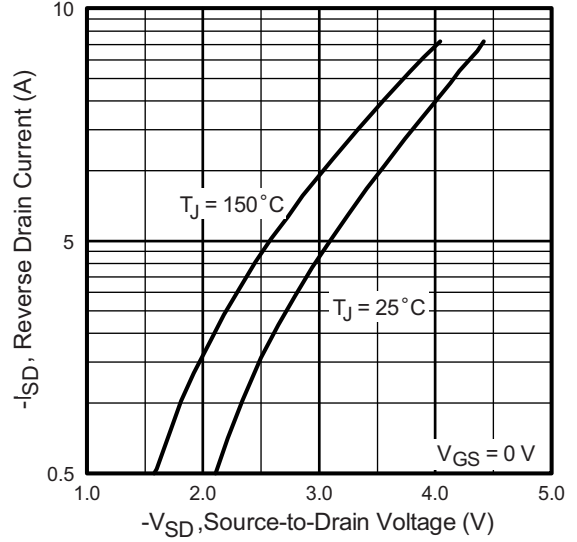


Fig. 7 - Typical Source-Drain Diode Forward Voltage

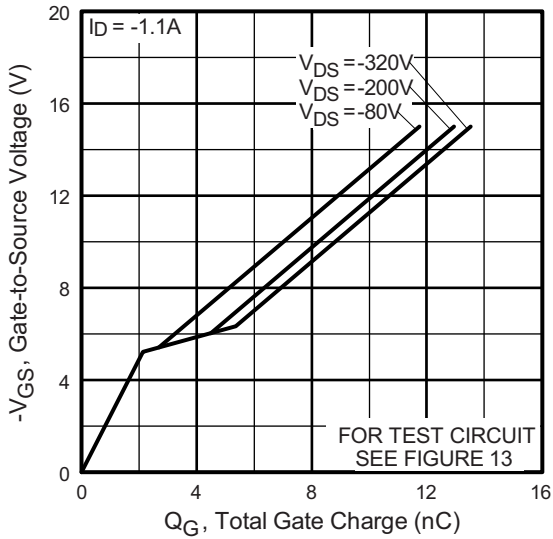


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

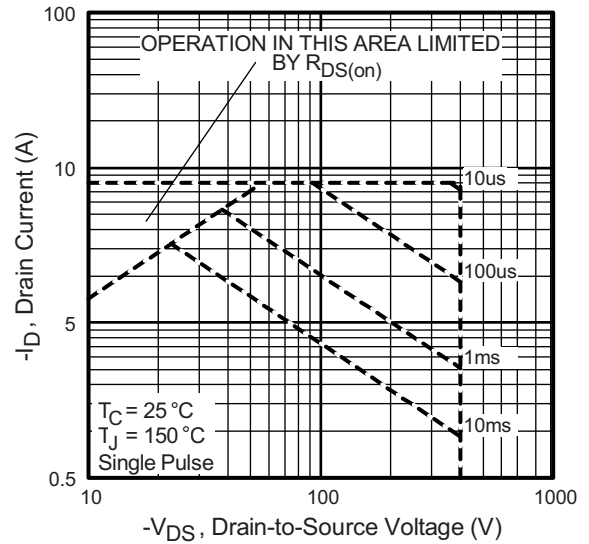


Fig. 8 - Maximum Safe Operating Area

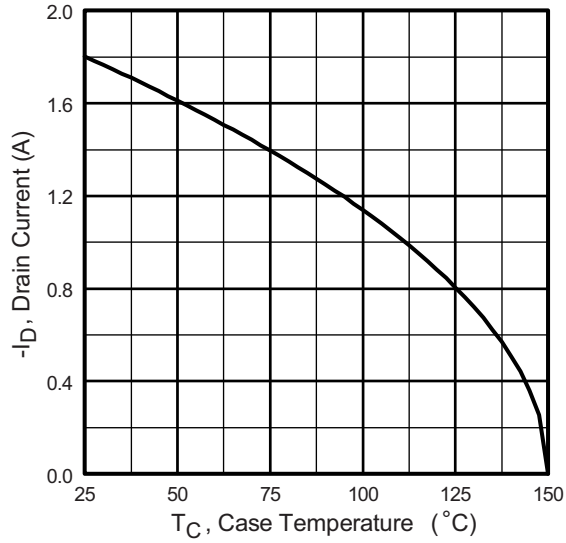


Fig. 9 - Maximum Drain Current vs. Case Temperature

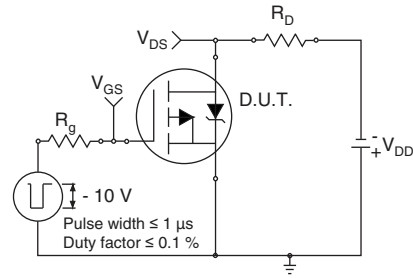


Fig. 10a - Switching Time Test Circuit

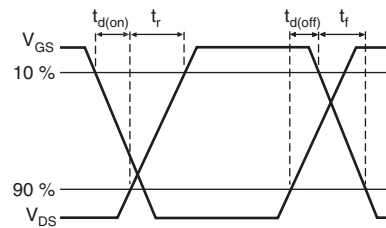


Fig. 10b - Switching Time Waveforms

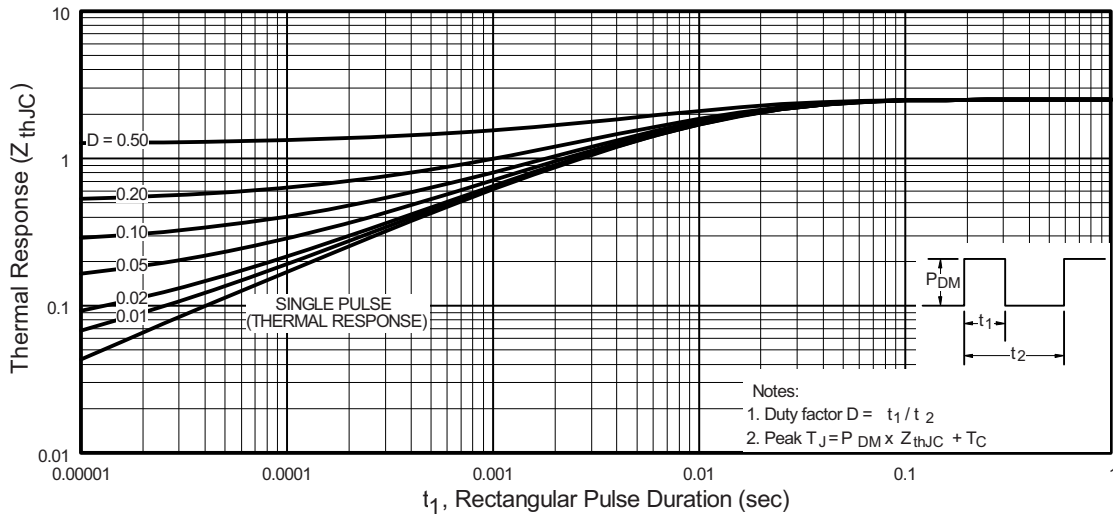


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

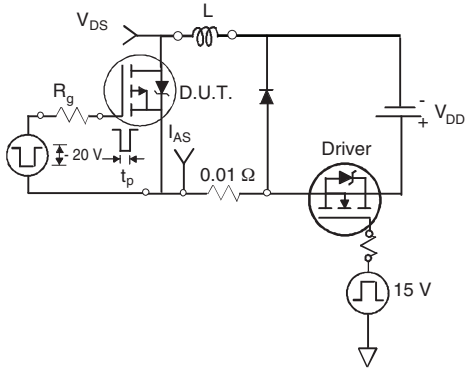


Fig. 12a - Unclamped Inductive Test Circuit

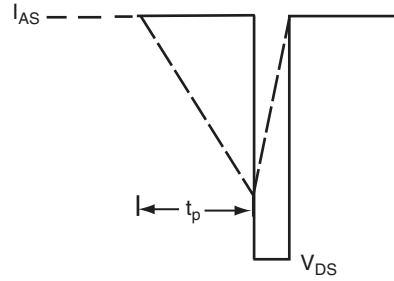


Fig. 12b - Unclamped Inductive Waveforms

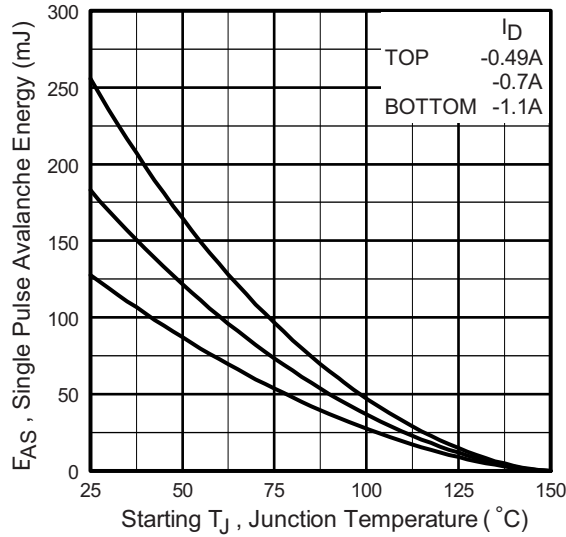


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

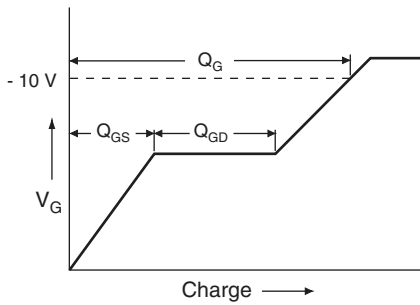


Fig. 13a - Basic Gate Charge Waveform

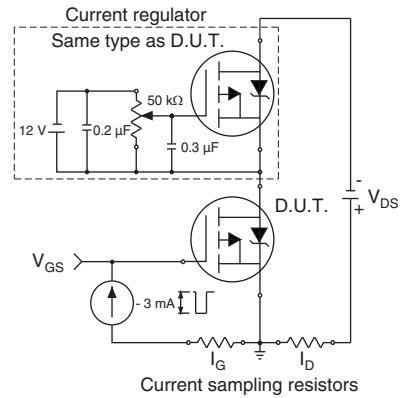
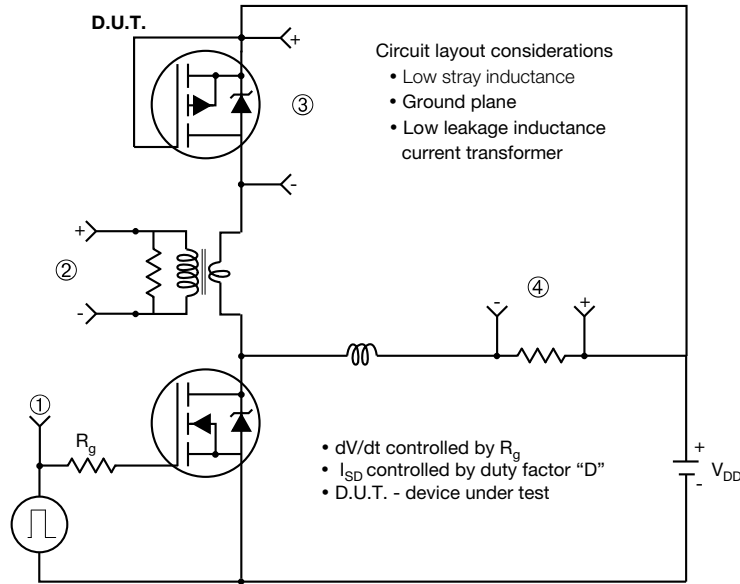
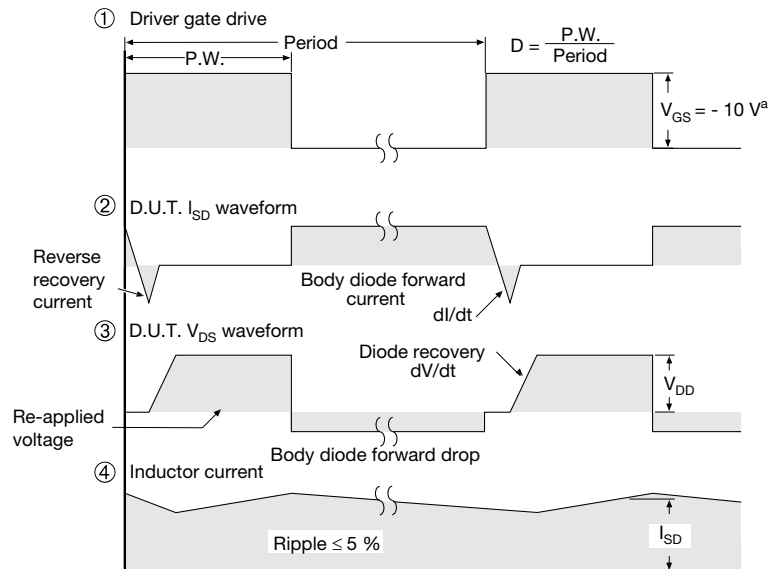


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

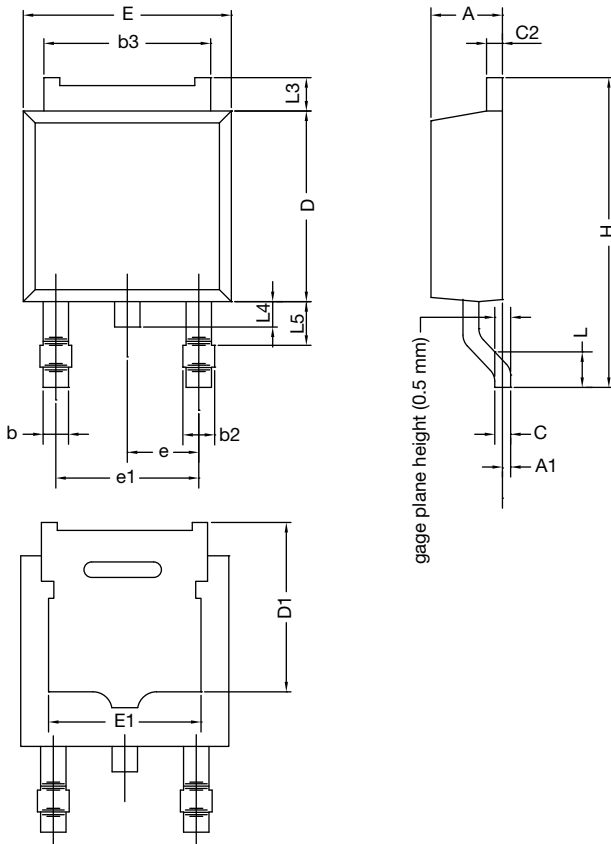


**Note**  
• Compliment N-Channel of D.U.T. for driver



**Fig. 14 - For P-Channel**

### TO-252AA Case Outline



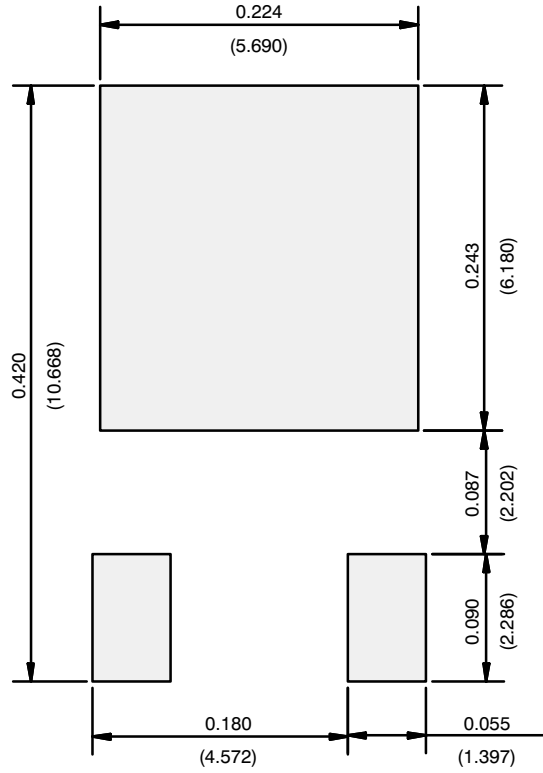
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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