

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	750	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.7
Q_g (Max.) (nC)	130	
Q_{gs} (nC)	17	
Q_{gd} (nC)	72	
Configuration	Single	

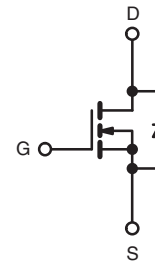
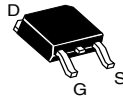
FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Isolated central mounting hole
- Fast switching
- Ease of paralleling
- Simple drive requirements



RoHS
COMPLIANT

DPAK
(TO-252)



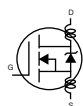

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	750	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current	V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	6.0	A
			$T_C = 100\text{ }^\circ\text{C}$	4.2	
Pulsed Drain Current ^a		I_{DM}	24		
Linear Derating Factor			1.2	$W/^\circ\text{C}$	
Single Pulse Avalanche Energy ^b		E_{AS}	490	mJ	
Repetitive Avalanche Current ^a		I_{AR}	5.4	A	
Repetitive Avalanche Energy ^a		E_{AR}	15	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	150	W	
Peak Diode Recovery dV/dt ^c		dV/dt	2.0	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) ^d	for 10 s		300		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 31\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 5.4\text{ A}$ (see fig. 12).
- $I_{SD} \leq 5.4\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq 600$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.83	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	750	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.98	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	μA
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.2\text{ A}^b$	-	1.7	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 3.2\text{ A}^b$	3.0	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	1900	-	pF
Output Capacitance	C_{oss}		-	470	-	
Reverse Transfer Capacitance	C_{rss}		-	280	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 5.4\text{ A}, V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	130	nC
Gate-Source Charge	Q_{gs}		-	-	17	
Gate-Drain Charge	Q_{gd}		-	-	72	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 5.4\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 75\text{ }\Omega$, see fig. 10 ^b	-	16	-	ns
Rise Time	t_r		-	36	-	
Turn-Off Delay Time	$t_{d(off)}$		-	100	-	
Fall Time	t_f		-	32	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	5.0	-	nH
Internal Source Inductance	L_S		-	13	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.4	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	22	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.4\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	550	830	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.4	3.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

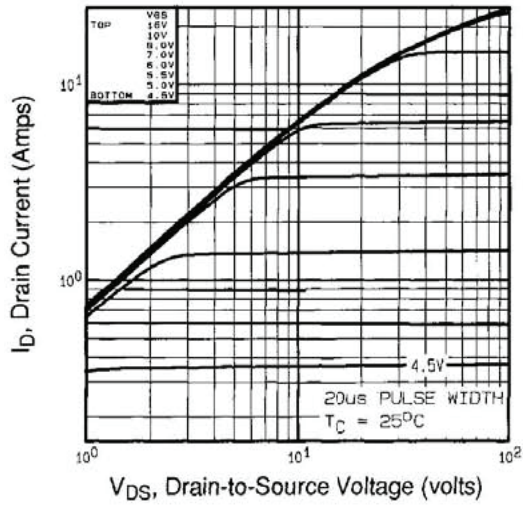


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

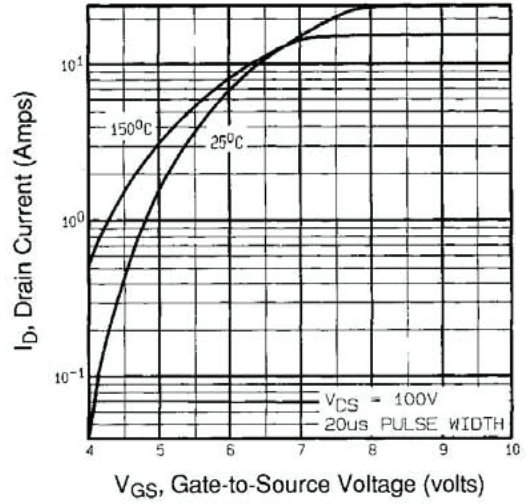


Fig. 3 - Typical Transfer Characteristics

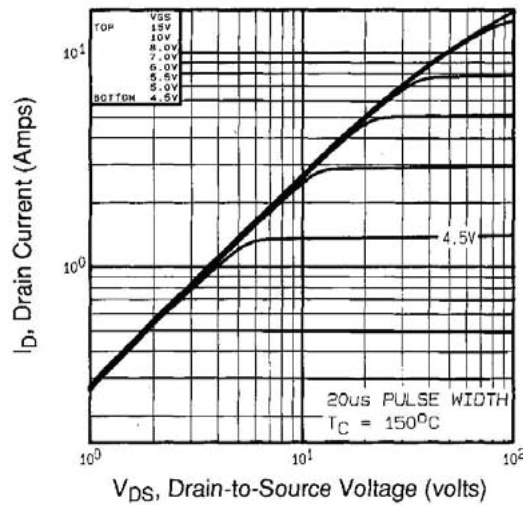


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

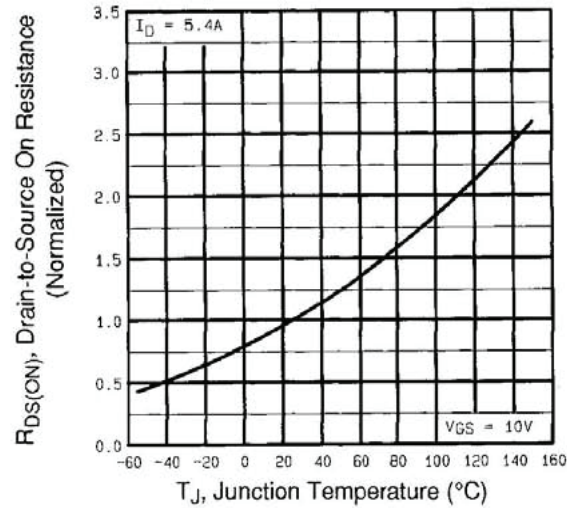


Fig. 4 - Normalized On-Resistance vs. Temperature

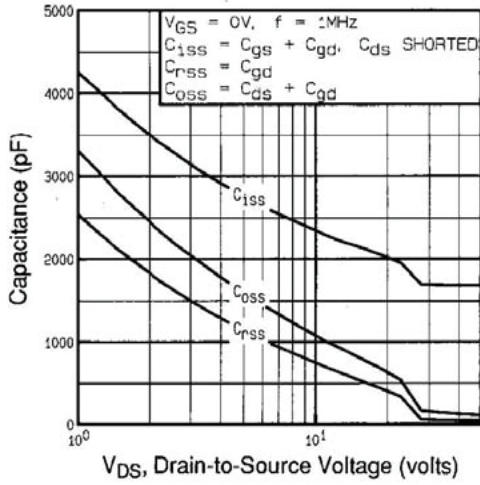


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

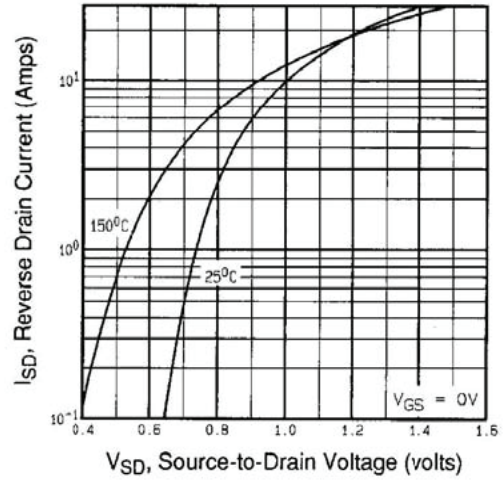


Fig. 7 - Typical Source-Drain Diode Forward Voltage

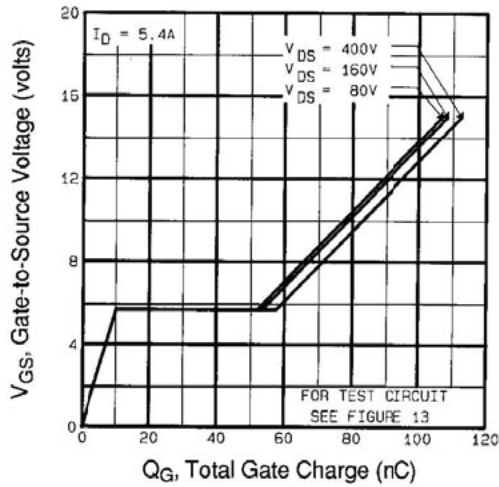


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

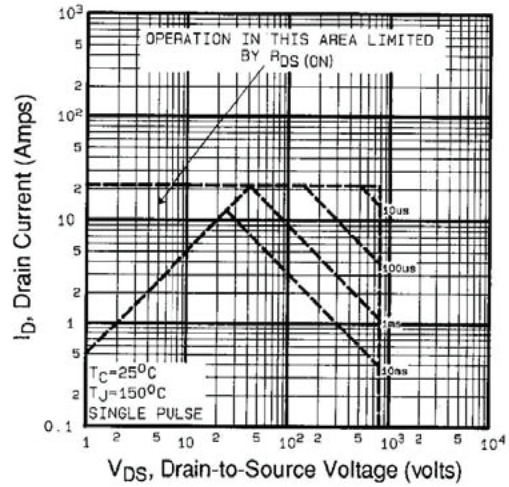


Fig. 8 - Maximum Safe Operating Area

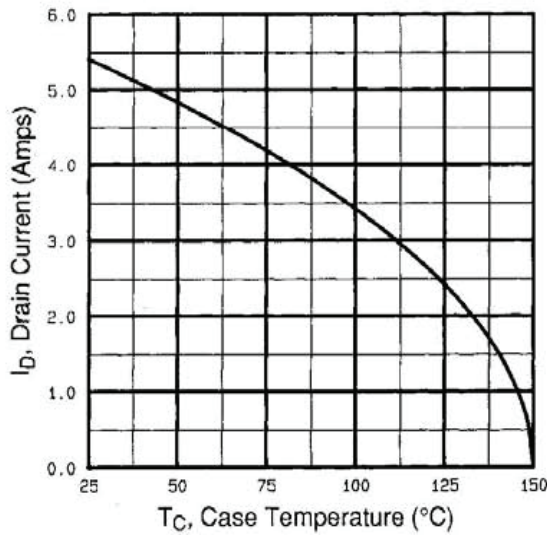


Fig. 9 - Maximum Drain Current vs. Case Temperature

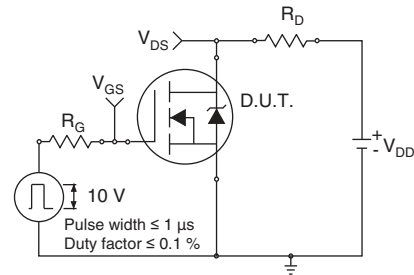


Fig. 10a - Switching Time Test Circuit

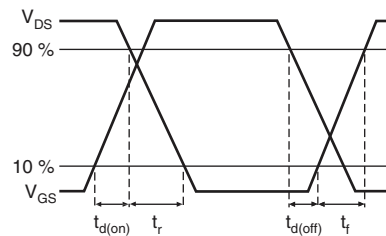


Fig. 10b - Switching Time Waveforms

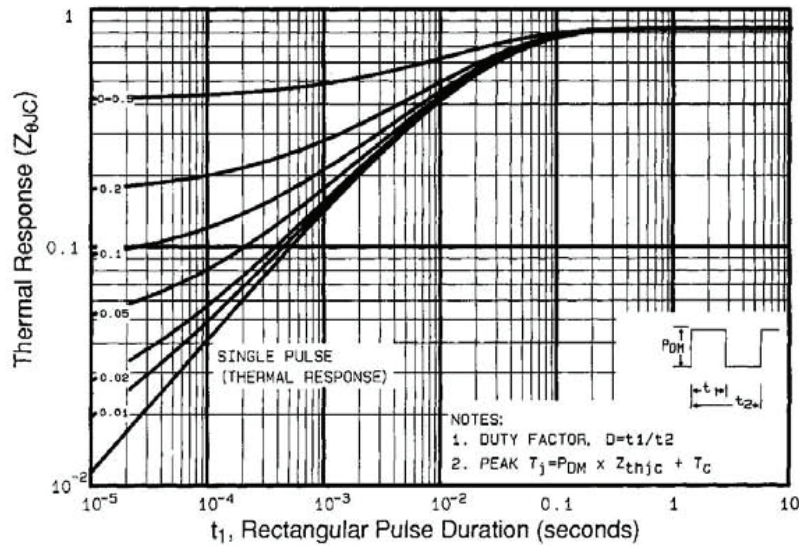


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

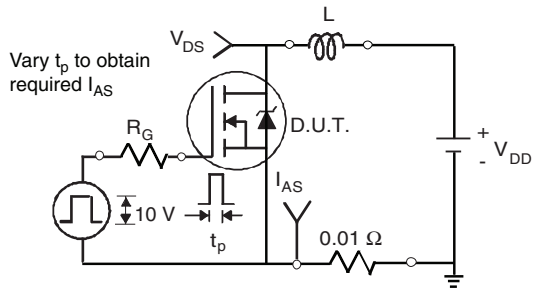


Fig. 12a - Unclamped Inductive Test Circuit

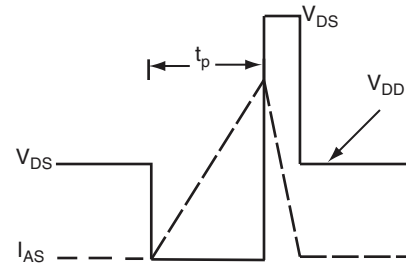


Fig. 12b - Unclamped Inductive Waveforms

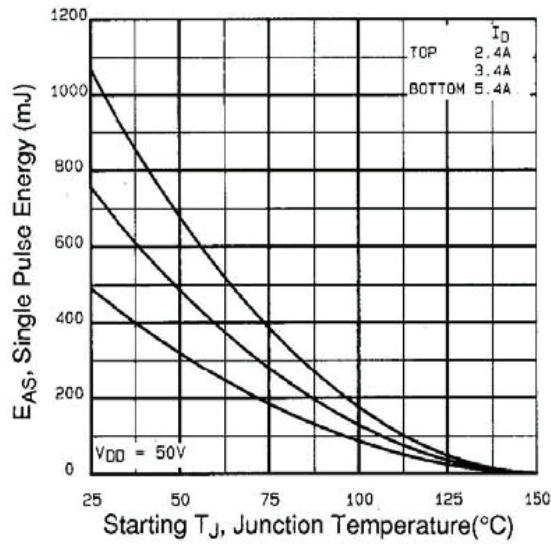


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

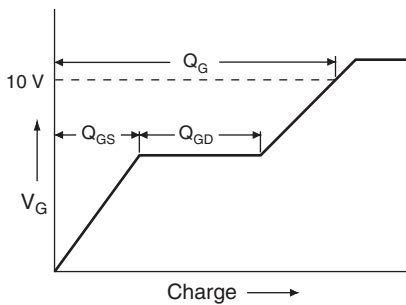


Fig. 13a - Basic Gate Charge Waveform

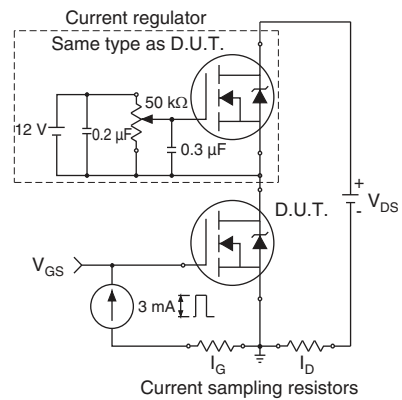
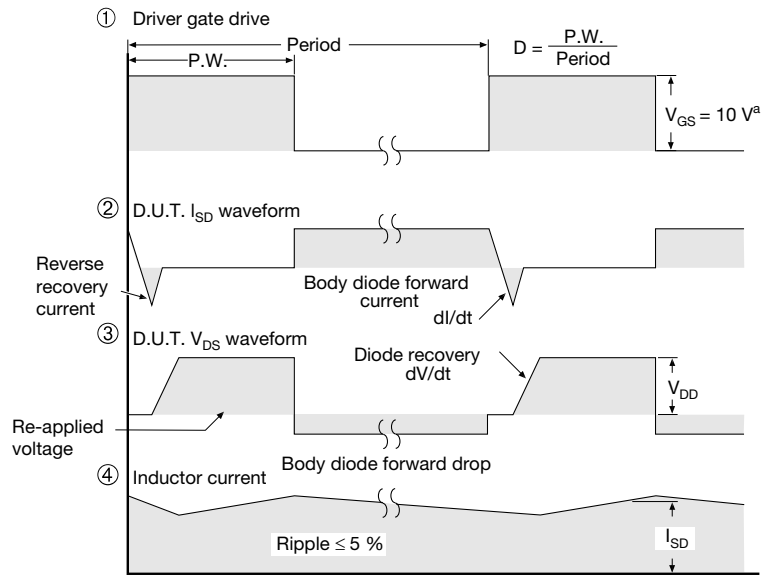
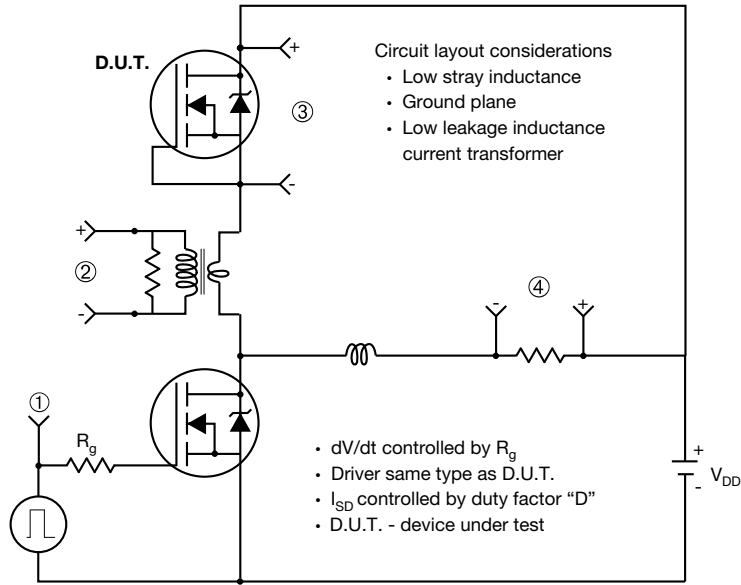


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

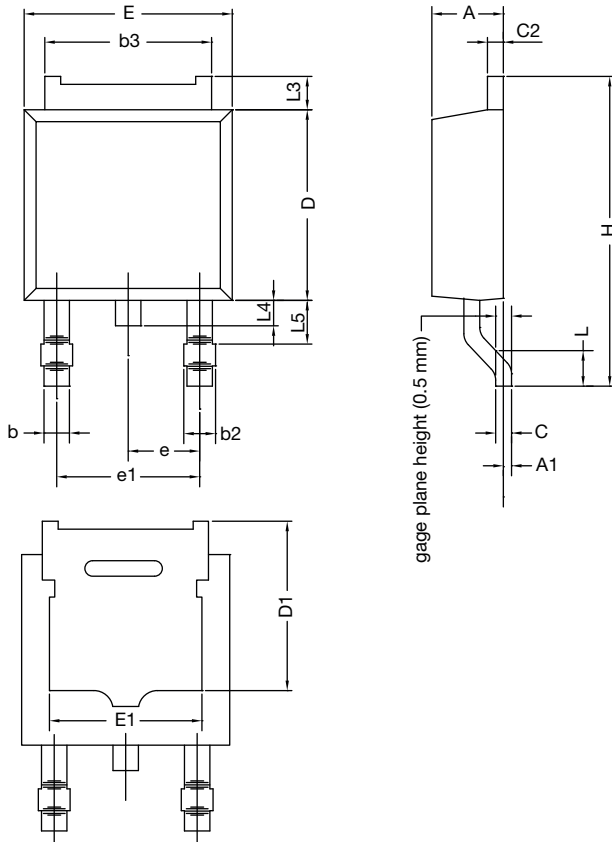


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-252AA Case Outline

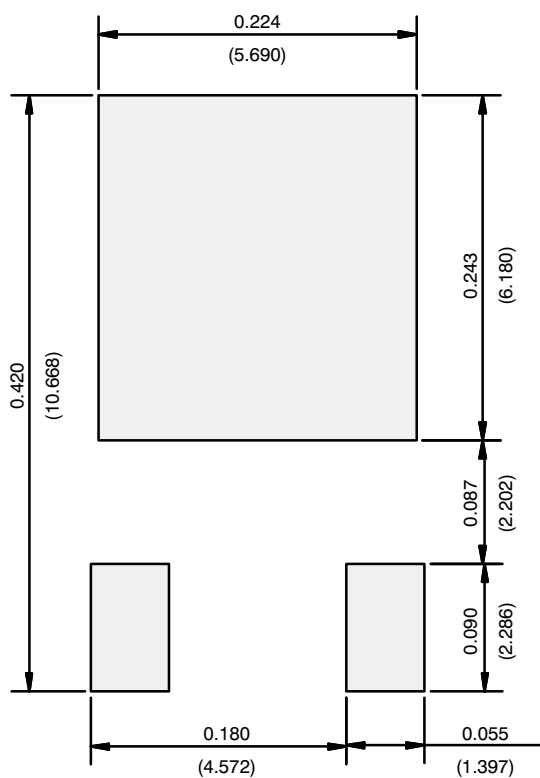


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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