

## N-Channel 250 V (D-S) MOSFET

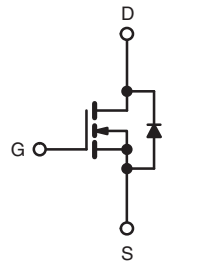
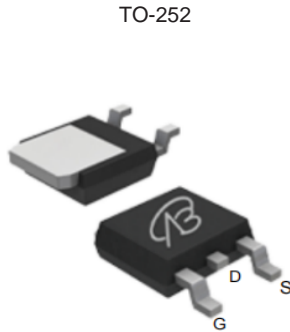
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	250	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	1.7
Q <sub>g</sub> (Max.) (nC)	8.0	
Q <sub>gs</sub> (nC)	1.6	
Q <sub>gd</sub> (nC)	4.3	
Configuration	Single	

### FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>		250	V
Gate-Source Voltage	V <sub>GS</sub>		± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	0.5	A
		T <sub>C</sub> = 100 °C	0.4	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>		1.5	W/°C
Linear Derating Factor			0.025	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.017	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>		50	mJ
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>		0.79	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>		0.31	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		3.1	W
	T <sub>A</sub> = 25 °C		2.0	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt		4.8	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		-55 to +150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300	



### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 128 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 0.79 A (see fig. 12).
- I<sub>SD</sub> ≤ 2.7 A, di/dt ≤ 65 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	-	40	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		250	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.39	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.47 A <sup>b</sup>	-	1.7	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 0.47 A		0.50	-	-	S
<b>Dynamic</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	170	-	pF
Output Capacitance	C <sub>oss</sub>			-	42	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	9.6	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 0.47 A, V <sub>DS</sub> = 200 V, see fig. 6 and 13 <sup>b</sup>	-	-	8.2	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	1.8	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	4.5	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 0.47 A, R <sub>g</sub> = 24 Ω, R <sub>D</sub> = 45 Ω, see fig. 10 <sup>b</sup>		-	7.0	-	ns
Rise Time	t <sub>r</sub>			-	7.6	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	16	-	
Fall Time	t <sub>f</sub>			-	7.0	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	0.5	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	1.5	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 0.6A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 1.8A, dI/dt = 100 A/μs <sup>b</sup>		-	70	-	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.64	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

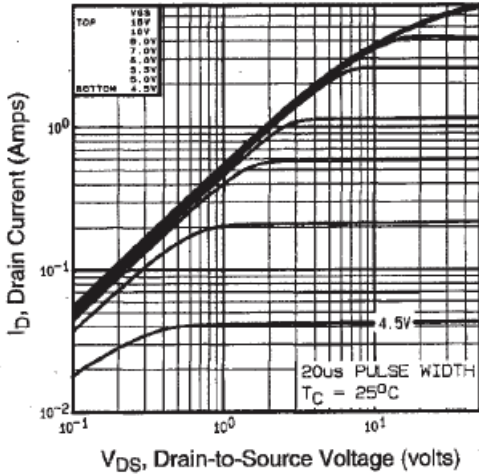


Fig. 1 - Typical Output Characteristics

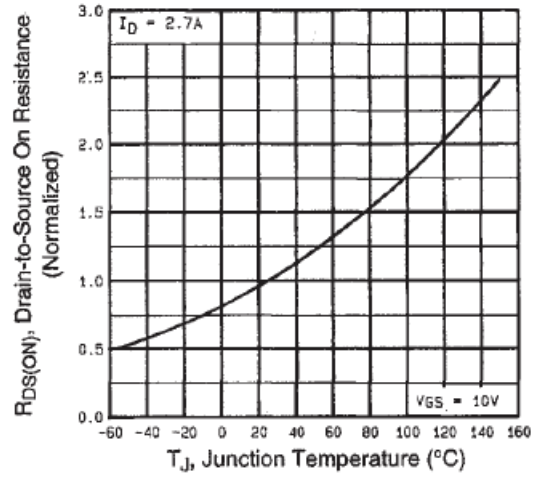


Fig. 4 - Normalized On-Resistance vs. Temperature

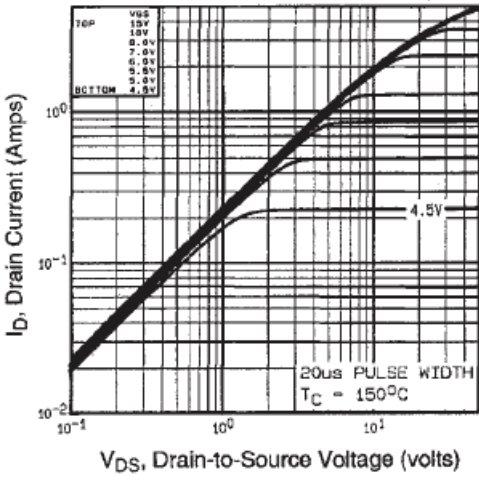


Fig. 2 - Typical Output Characteristics

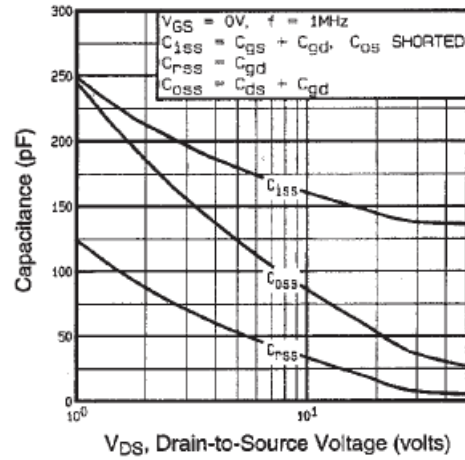


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

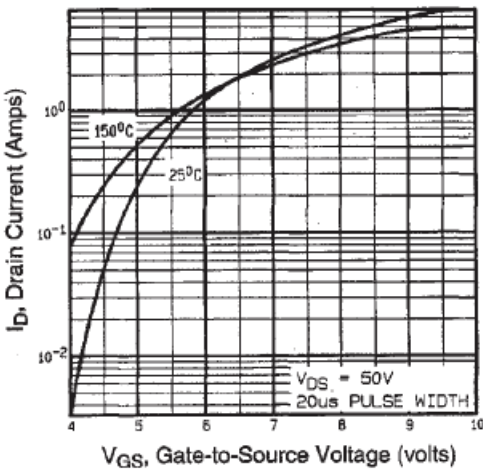


Fig. 3 - Typical Transfer Characteristics

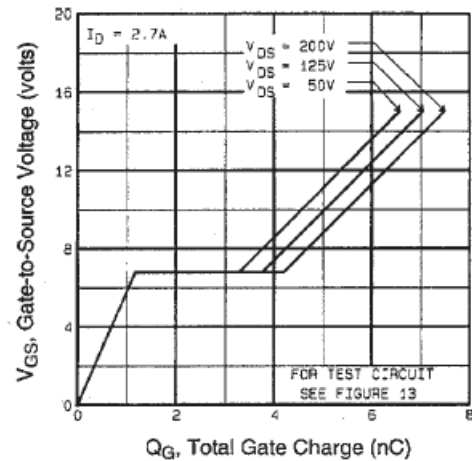


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

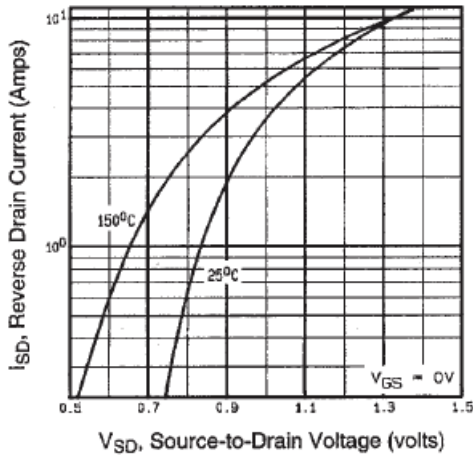


Fig. 7 - Typical Source-Drain Diode Forward Voltage

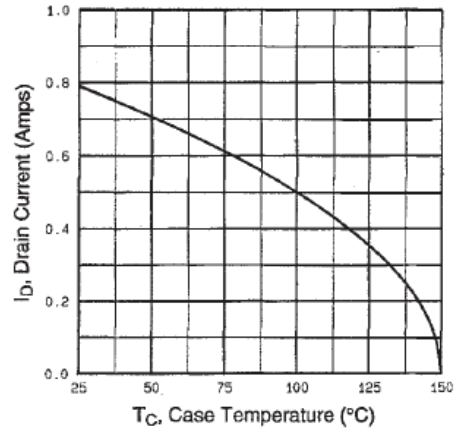


Fig. 9 - Maximum Drain Current vs. Case Temperature

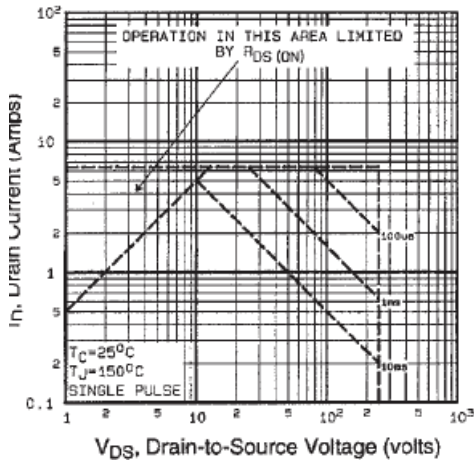


Fig. 8 - Maximum Safe Operating Area

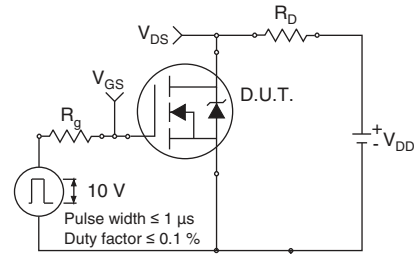


Fig. 10a - Switching Time Test Circuit

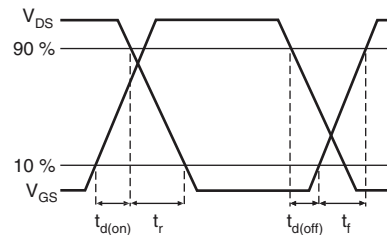


Fig. 10b - Switching Time Waveforms

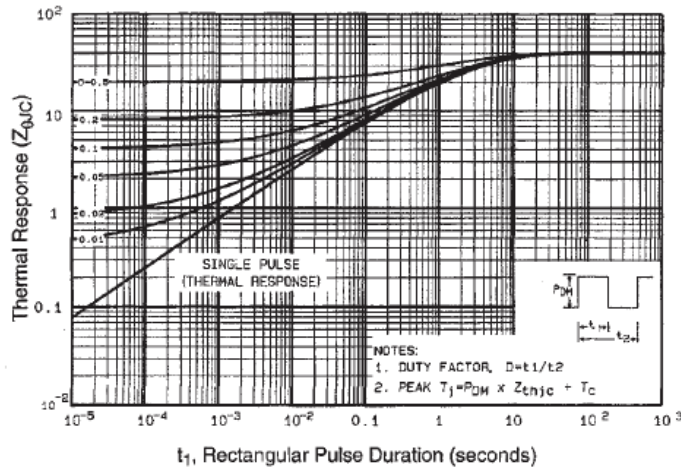


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

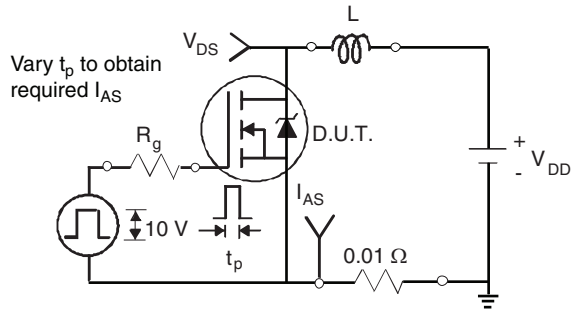


Fig. 12a - Unclamped Inductive Test Circuit

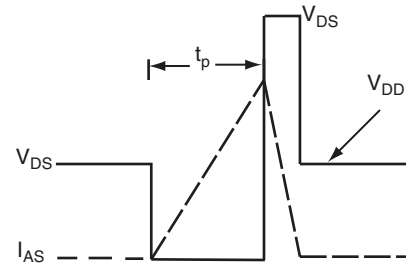


Fig. 12b - Unclamped Inductive Waveforms

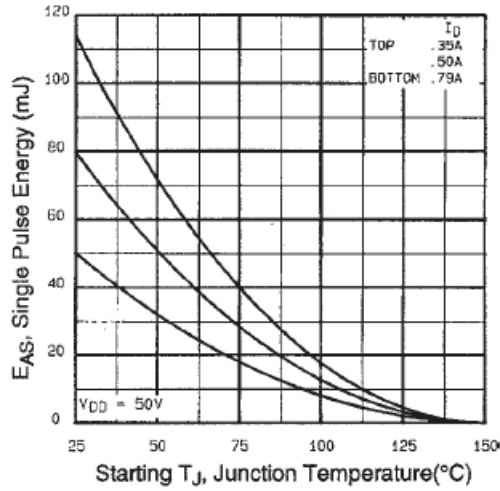


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

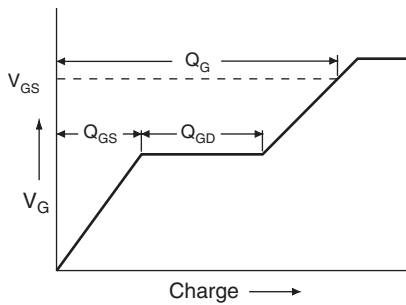


Fig. 13a - Basic Gate Charge Waveform

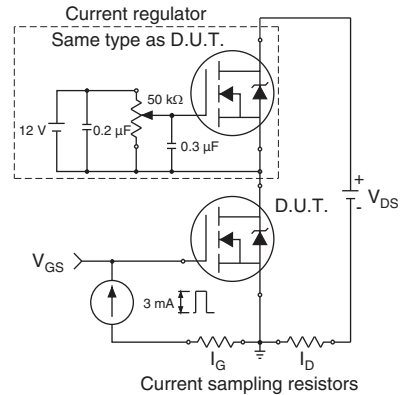
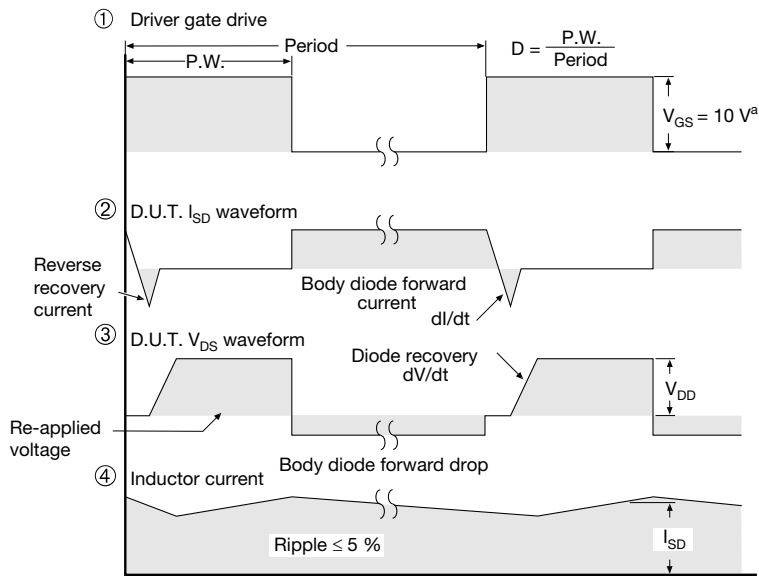
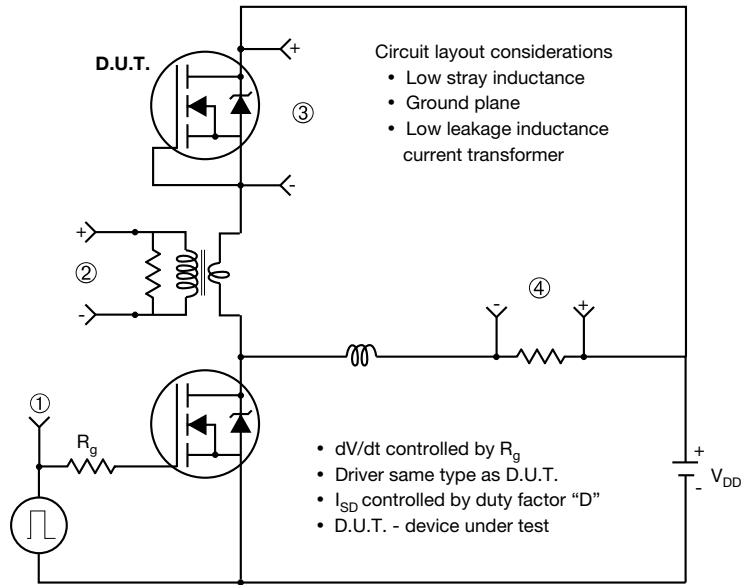


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

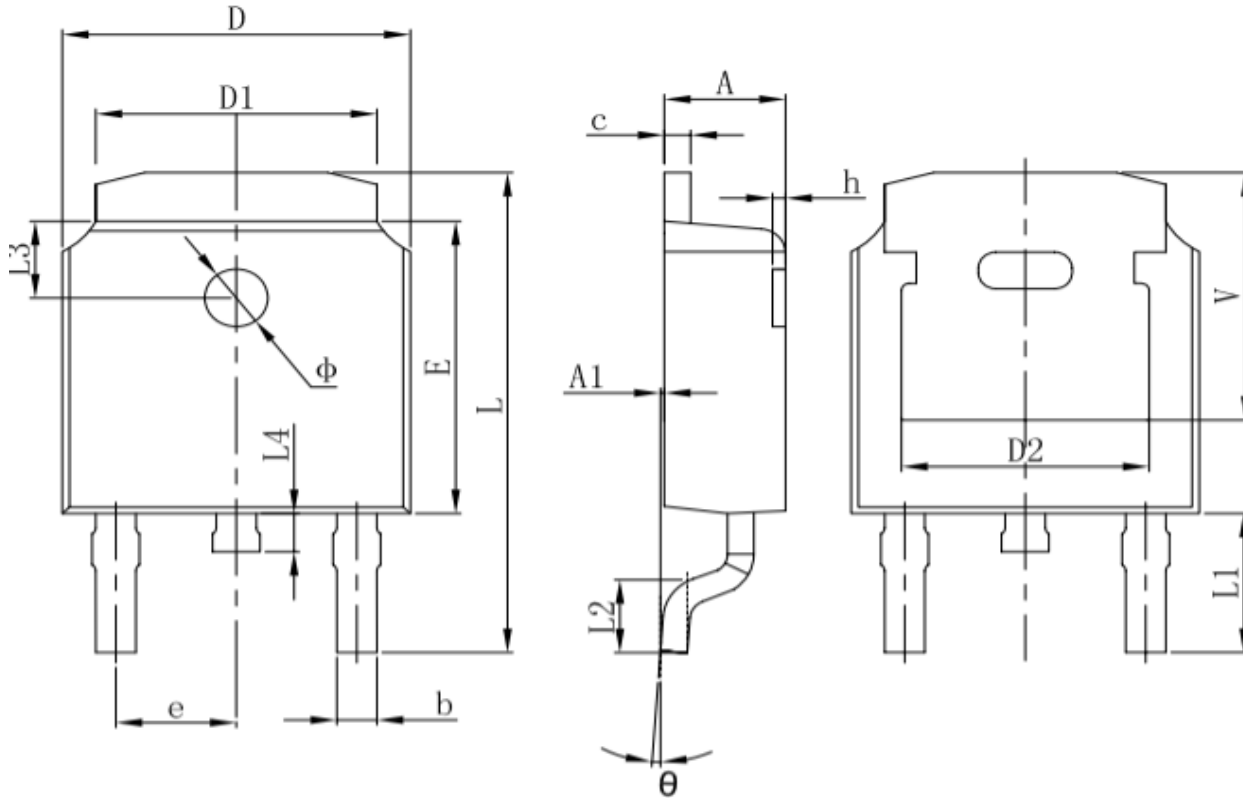


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig.14 - For N-Channel**

## TO252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

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