

N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (TYP.)
30	0.016 at V _{GS} = 10 V	9	9 nC
	0.019 at V _{GS} = 4.5 V	8	

FEATURES

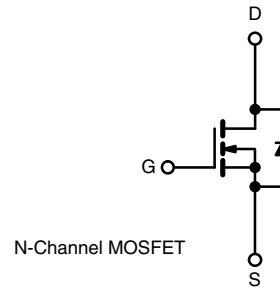
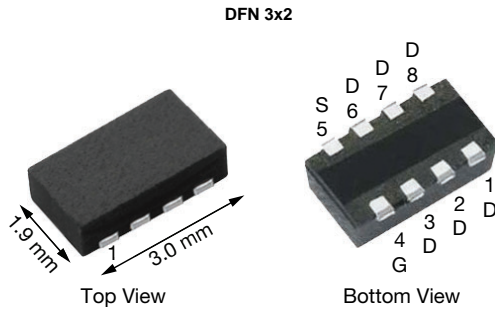
- TrenchFET® power MOSFET

APPLICATIONS

- Load switches
- Notebook PC



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	9
		T _C = 70 °C	6 ^a
		T _A = 25 °C	6 ^{a, b, c}
		T _A = 70 °C	6 ^{a, b, c}
Pulsed Drain Current	I _{DM}	30	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	2.1 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	6.3
		T _C = 70 °C	4
		T _A = 25 °C	2.5 ^{b, c}
		T _A = 70 °C	1.6 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{a, c, d}	R _{thJA}	40	50	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	15	20	

Notes

- Package limited, T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s
- Maximum under steady state conditions is 95 °C/W.
- The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

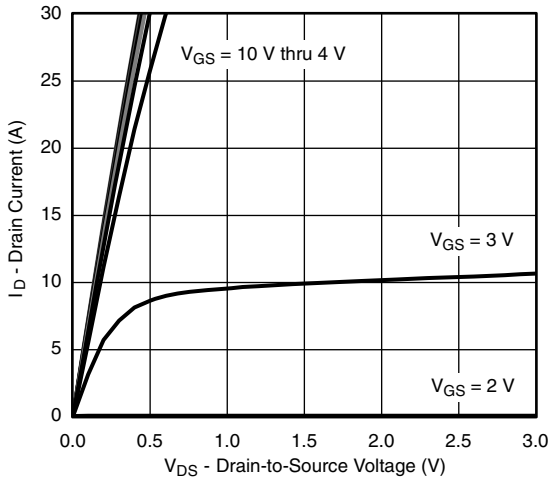
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	31	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.1	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2	-	2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9.1\text{ A}$	-	0.016	-	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8.1\text{ A}$	-	0.019	-	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9.1\text{ A}$	-	30	-	S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1200	-	pF
Output Capacitance	C_{oss}		-	180	-	
Reverse Transfer Capacitance	C_{rss}		-	80	-	
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 9.1\text{ A}$	-	19	29	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.1\text{ A}$	-	9	14	
Gate-Source Charge	Q_{gs}		-	3.5	-	
Gate-Drain Charge	Q_{gd}		-	2.3	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$	-	3	-	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.1\text{ }\Omega$ $I_D \cong 7.3\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	20	30	ns
Rise Time	t_r		-	12	20	
Turn-Off Delay Time	$t_{d(off)}$		-	20	30	
Fall Time	t_f		-	10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.1\text{ }\Omega$ $I_D \cong 7.3\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	10	15	
Rise Time	t_r		-	10	15	
Turn-Off Delay Time	$t_{d(off)}$		-	20	30	
Fall Time	t_f		-	10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	5.2	A
Pulse Diode Forward Current	I_{SM}		-	-	30	
Body Diode Voltage	V_{SD}	$I_S = 7.3\text{ A}, V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 7.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	-	20	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	10	20	nC
Reverse Recovery Fall Time	t_a		-	11	-	ns
Reverse Recovery Rise Time	t_b		-	9	-	

Notes

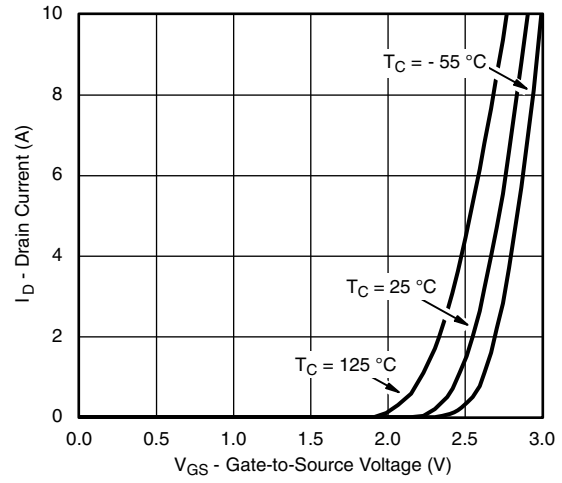
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

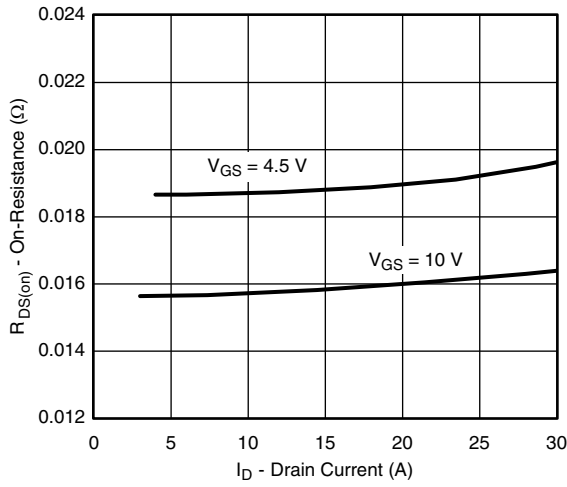
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



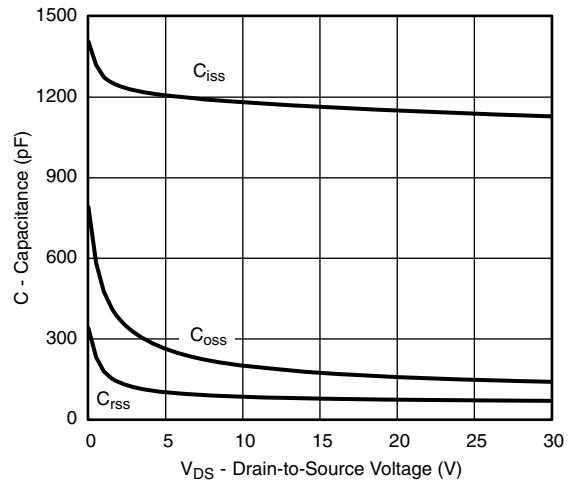
Output Characteristics



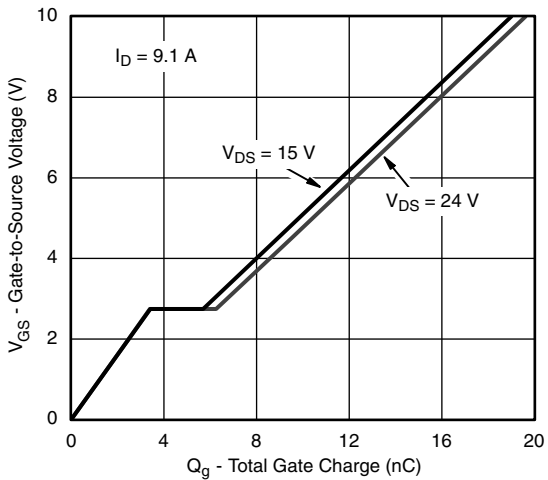
Transfer Characteristics



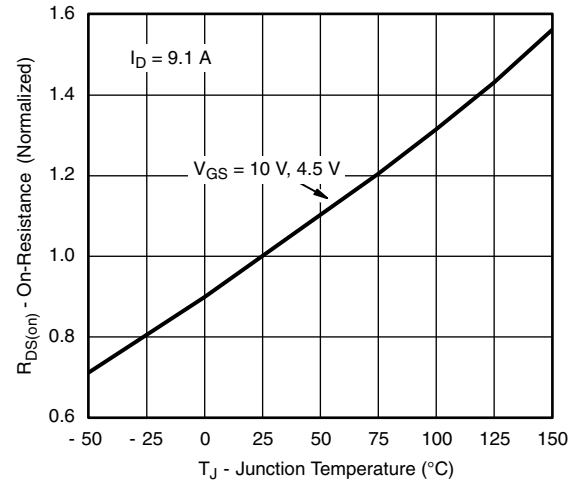
On-Resistance vs. Drain Current



Capacitance

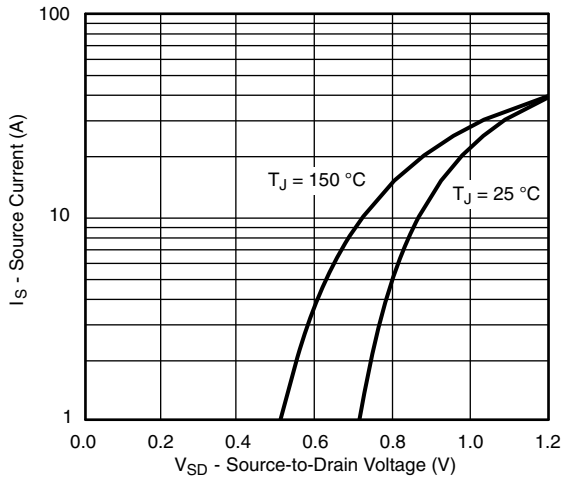


Gate Charge

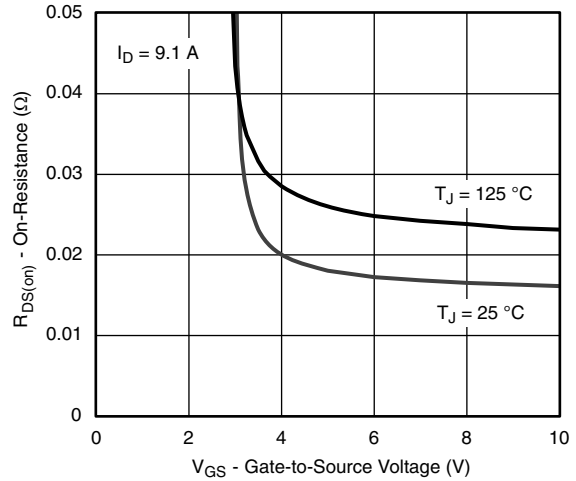


On-Resistance vs. Junction Temperature

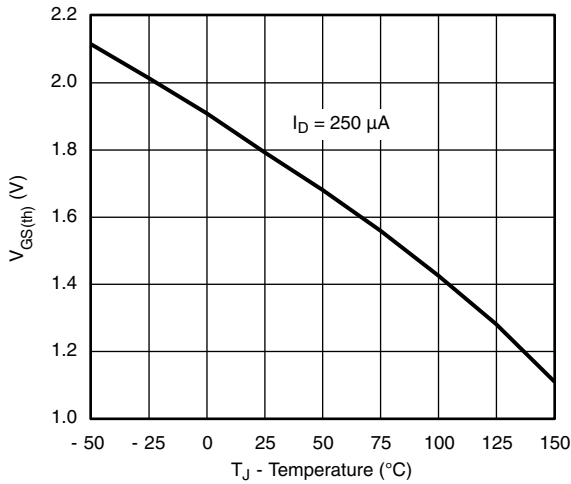
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



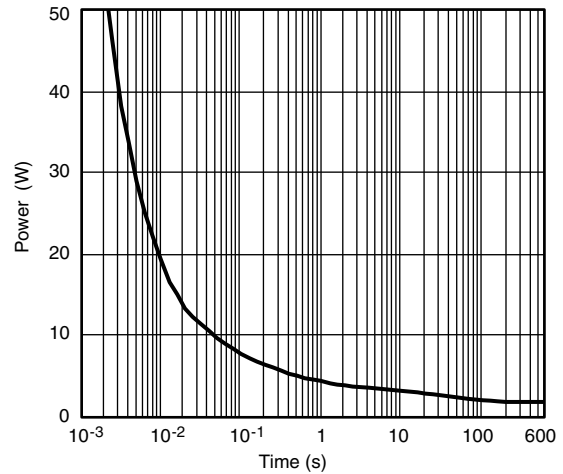
Source-Drain Diode Forward Voltage



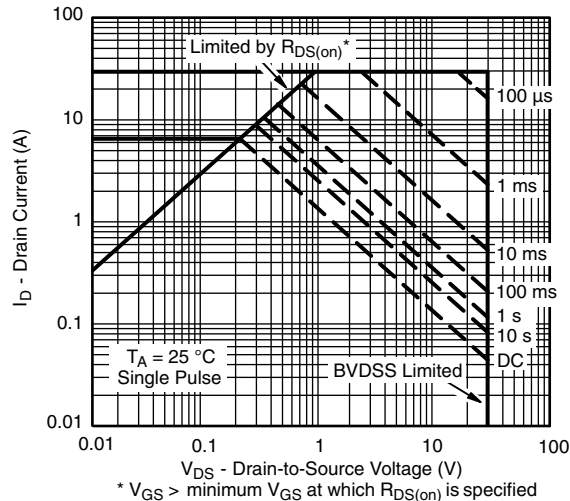
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



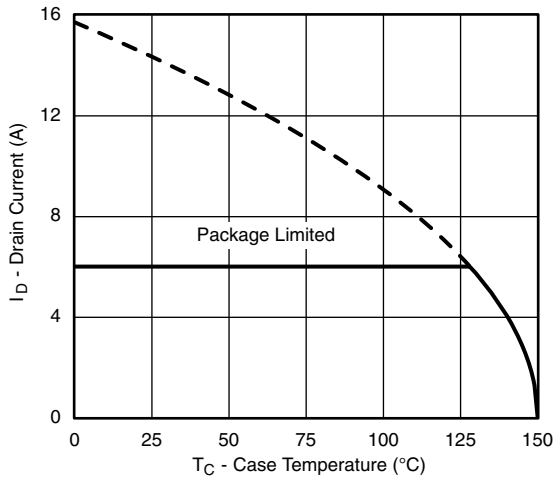
Single Pulse Power



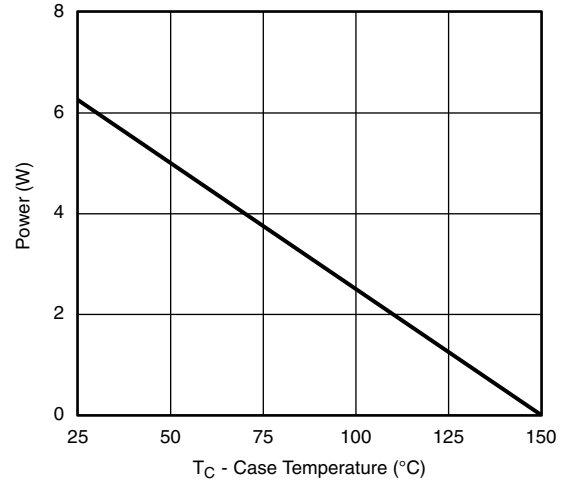
Safe Operating Area, Junction-to-Ambient

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a

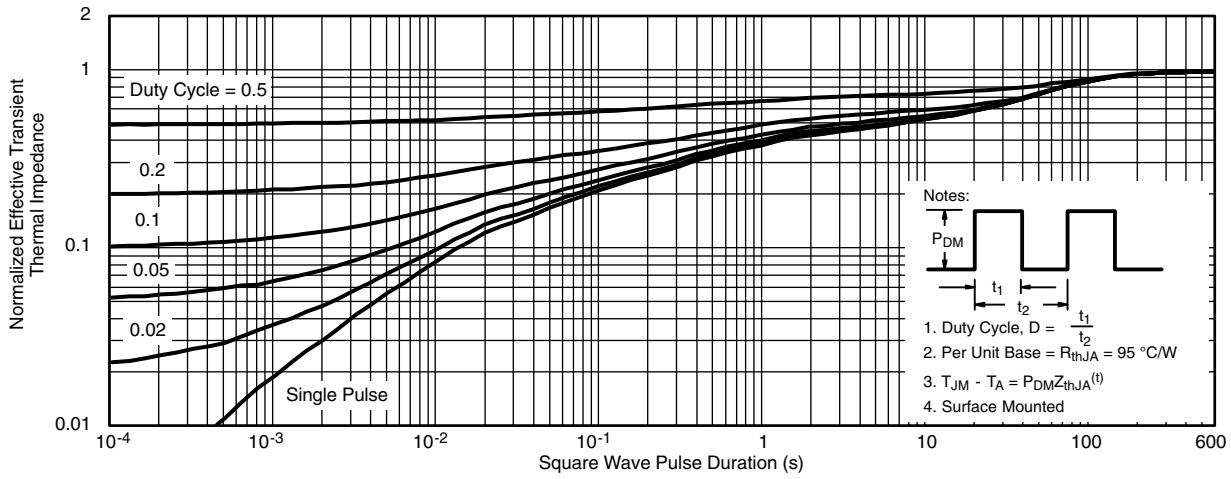


Power Derating

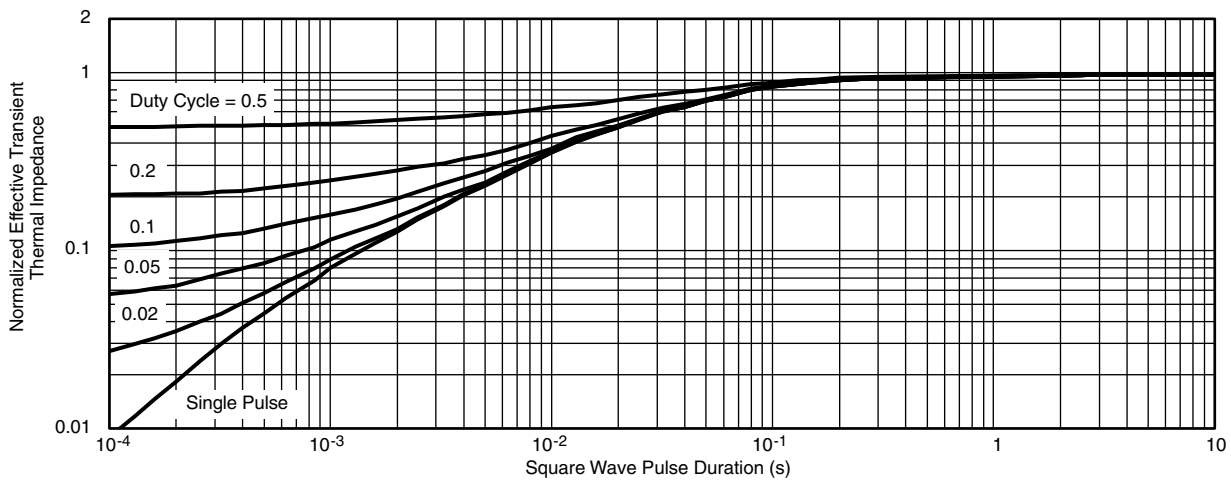
Note

- a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

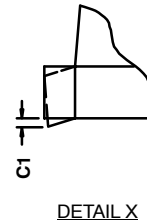
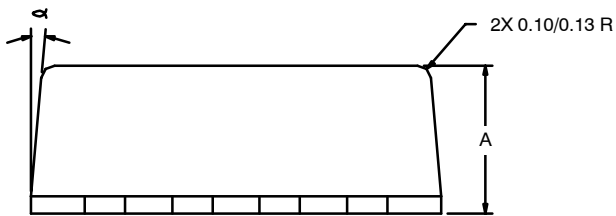
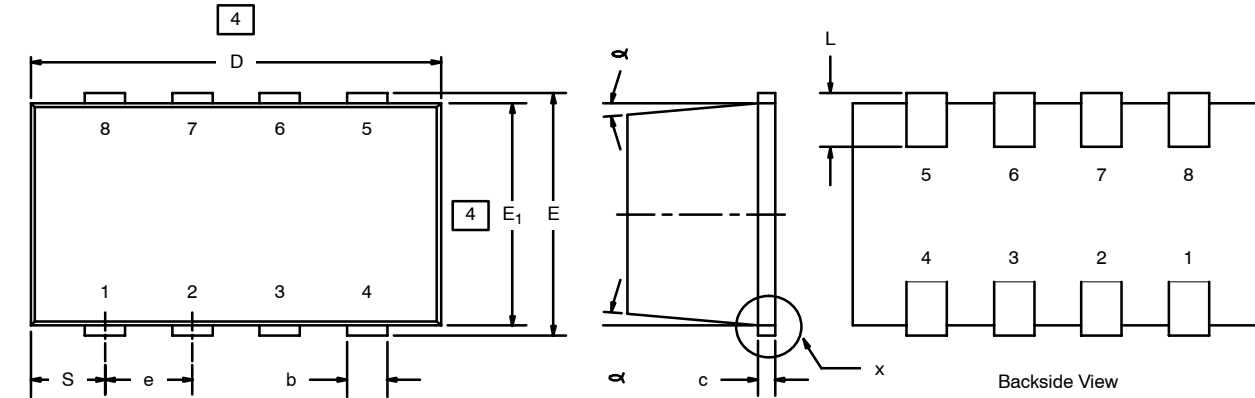


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

DFN 3x2



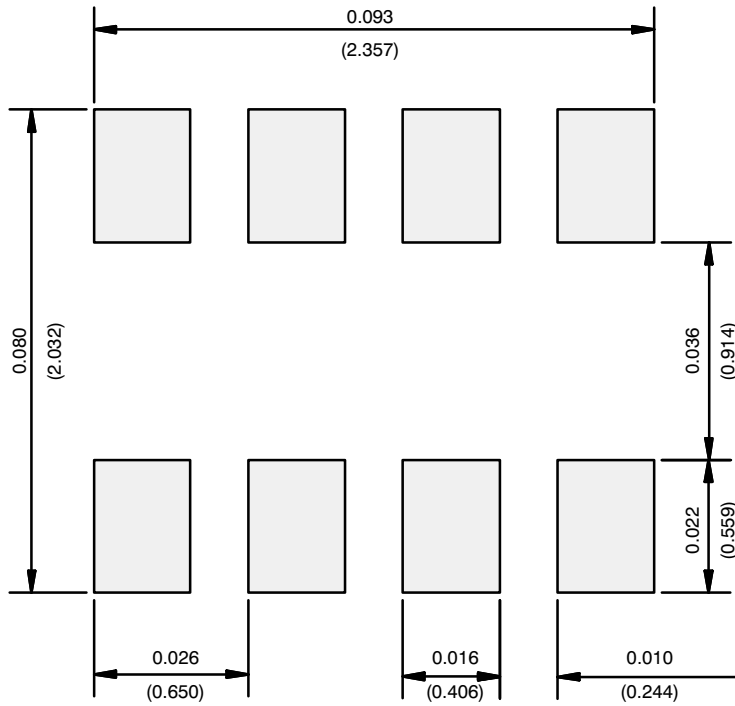
NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.

4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	-	1.10	0.039	-	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	-	0.038	0	-	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	-	0.42	0.011	-	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

RECOMMENDED MINIMUM PADS FOR DFN3x2



Recommended Minimum Pads
Dimensions in Inches/(mm)

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