

F3710S-VB Datasheet

Power MOSFET

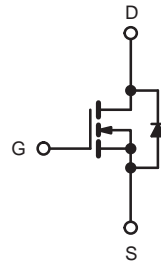
| PRODUCT SUMMARY | | |
|----------------------------|------------------------|-------|
| V _{DS} (V) | 100 | |
| R _{DS(on)} (Ω) | V _{GS} = 10 V | 0.020 |
| Q _g (Max.) (nC) | 70 | |
| Q _{gs} (nC) | 13 | |
| Q _{gd} (nC) | 39 | |
| Configuration | Single | |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|-------------------------|------------------|------|
| PARAMETER | SYMBOL | | LIMIT | UNIT |
| Drain-Source Voltage | V _{DS} | | 100 | V |
| Gate-Source Voltage | V _{GS} | | ±20 | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 25 °C | 70 | A |
| | | T _C = 100 °C | 56 | |
| Pulsed Drain Current ^{a, e} | I _{DM} | | 250 | |
| Linear Derating Factor | | | 1.0 | W/°C |
| Single Pulse Avalanche Energy ^{b, e} | E _{AS} | | 580 | mJ |
| Avalanche Current ^a | I _{AR} | | 20 | A |
| Repetitive Avalanche Energy ^a | E _{AR} | | 13 | mJ |
| Maximum Power Dissipation | T _C = 25 °C | | 3.1 | W |
| | T _A = 25 °C | | 130 | |
| Peak Diode Recovery dV/dt ^{c, e} | dV/dt | | 5.0 | V/ns |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | 300 ^d | |

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 50 V, starting T_J = 25 °C, L = 2.7 mH, R_g = 25 Ω, I_{AS} = 18 A (see fig. 12).
- I_{SD} ≤ 20 A, di/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient (PCB Mounted, Steady-State) ^a | R_{thJA} | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|--|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 100 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^c$ | | - | 0.29 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 11\text{ A}^b$ | - | 0.020 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 11\text{ A}^d$ | | 6.7 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$, see fig. 5 ^d | | - | 1300 | - | pF |
| Output Capacitance | C_{oss} | | | - | 430 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 130 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}, V_{DS} = 160\text{ V},$ see fig. 6 and 13 ^{b, c} | - | - | 70 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 13 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 39 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, I_D = 20\text{ A},$ $R_g = 9.1\text{ }\Omega, R_D = 5.4\text{ }\Omega$, see fig. 10 ^{b, c} | | - | 14 | - | ns |
| Rise Time | t_r | | | - | 51 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 45 | - | |
| Fall Time | t_f | | | - | 36 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 20 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 72 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 20\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 2.0 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b, c$ | | - | 300 | 610 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 3.4 | 7.1 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
 c. Uses IRF640/SiHF640 data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

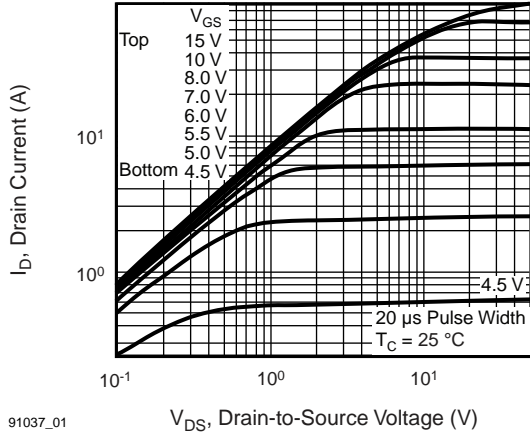


Fig. 1 - Typical Output Characteristics, $T_J = 25\text{ °C}$

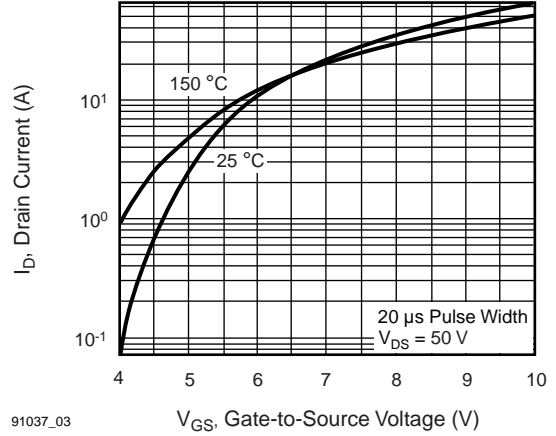


Fig. 3 - Typical Transfer Characteristics

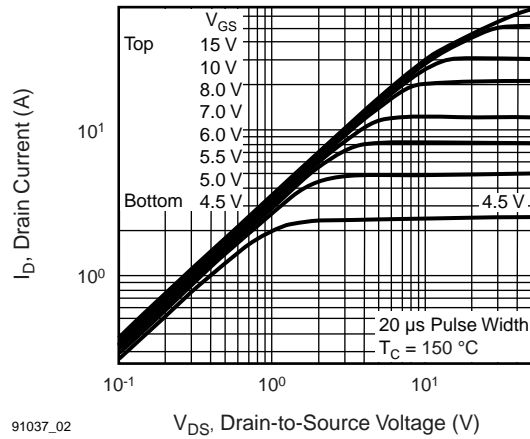


Fig. 2 - Typical Output Characteristics, $T_J = 175\text{ °C}$

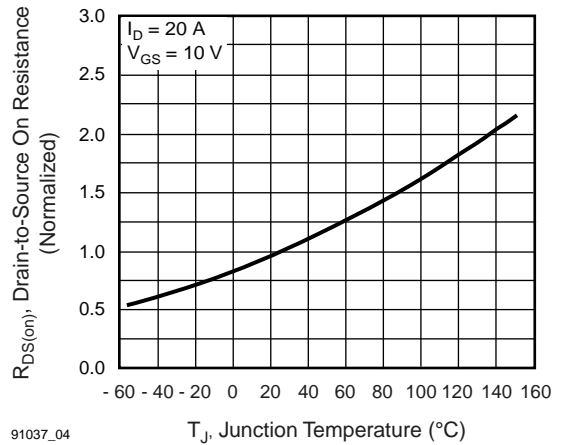
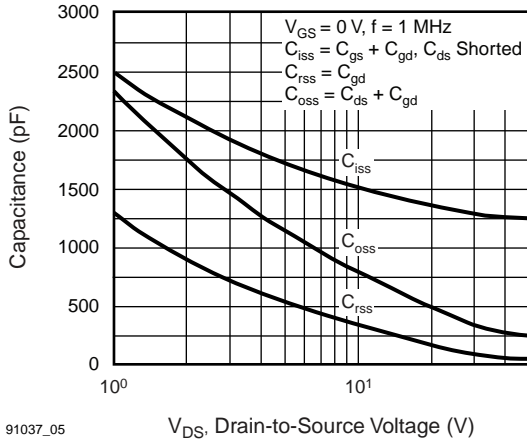
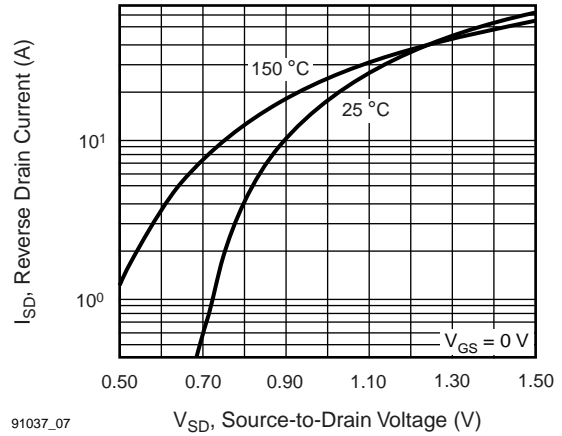


Fig. 4 - Normalized On-Resistance vs. Temperature



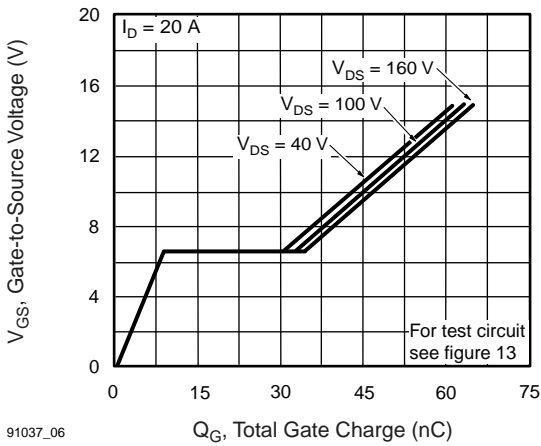
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



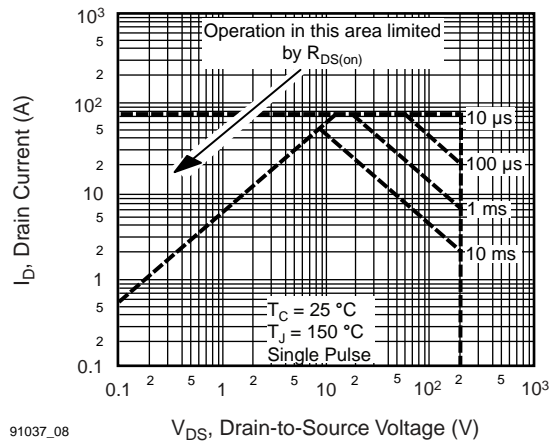
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area

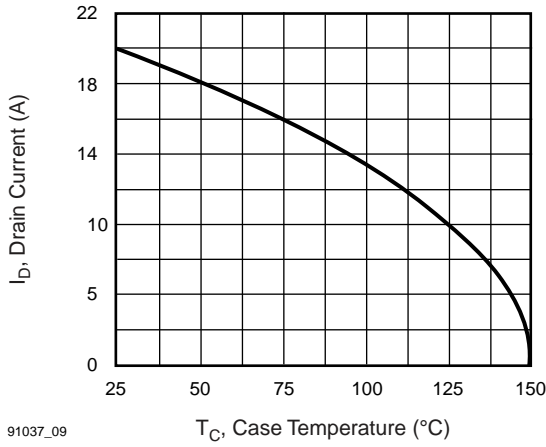


Fig. 9 - Maximum Drain Current vs. Case Temperature

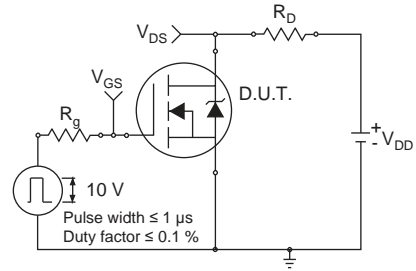


Fig. 10a - Switching Time Test Circuit

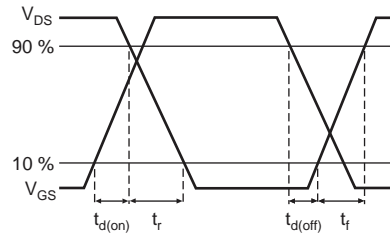


Fig. 10b - Switching Time Waveforms

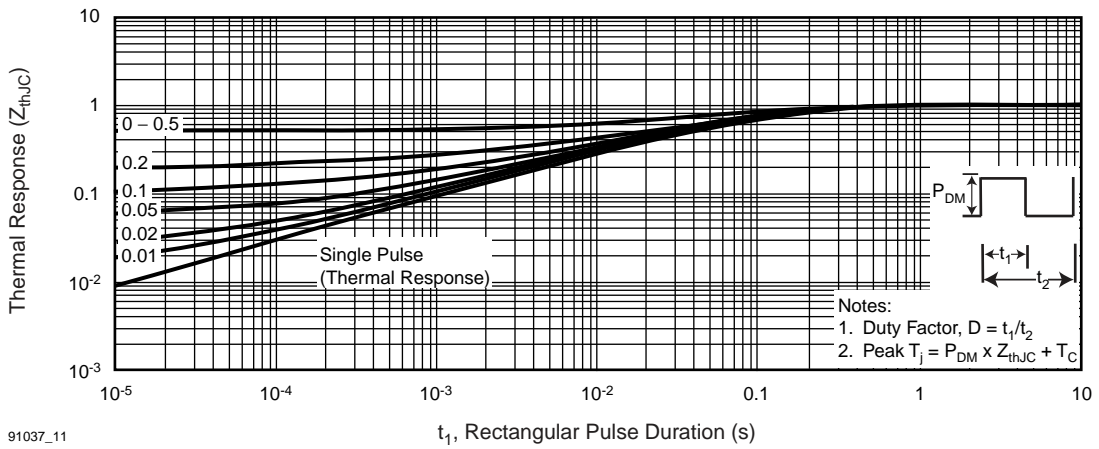


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

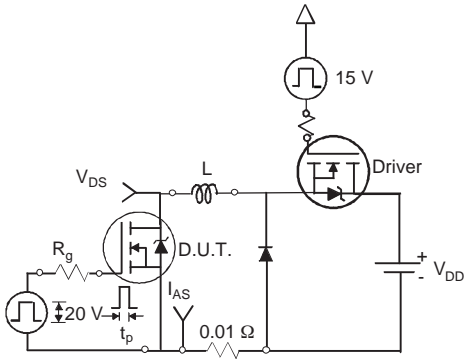


Fig. 12a - Unclamped Inductive Test Circuit

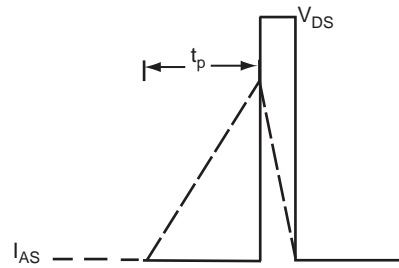


Fig. 12b - Unclamped Inductive Waveforms

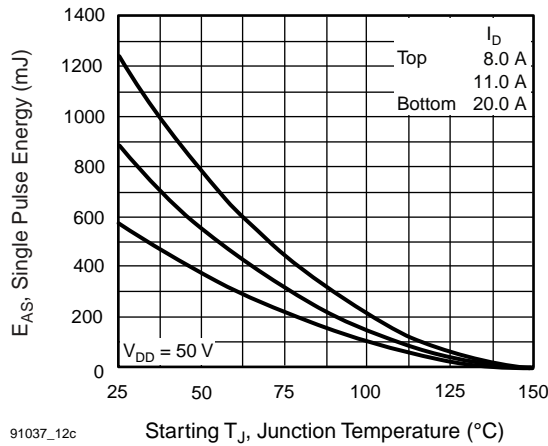


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

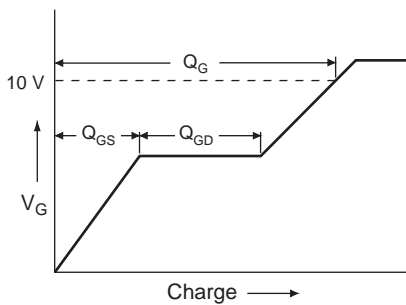


Fig. 13a - Basic Gate Charge Waveform

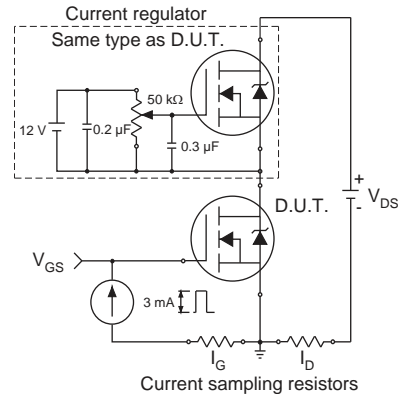
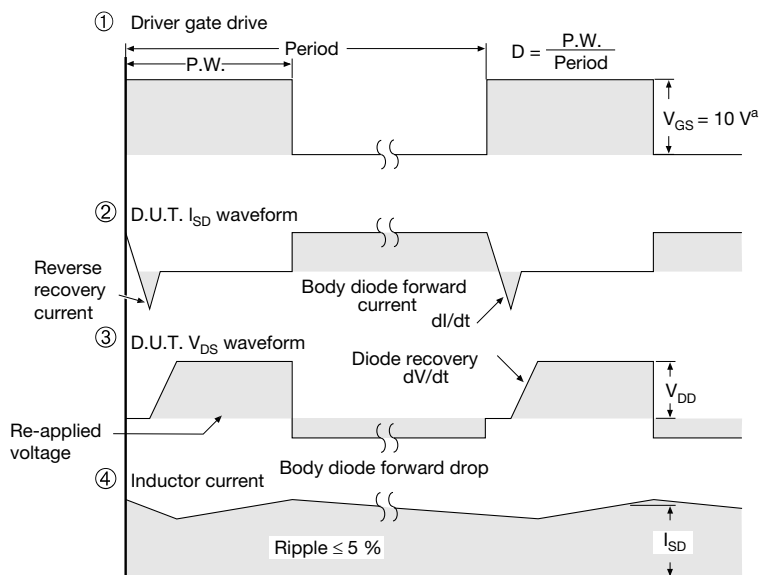
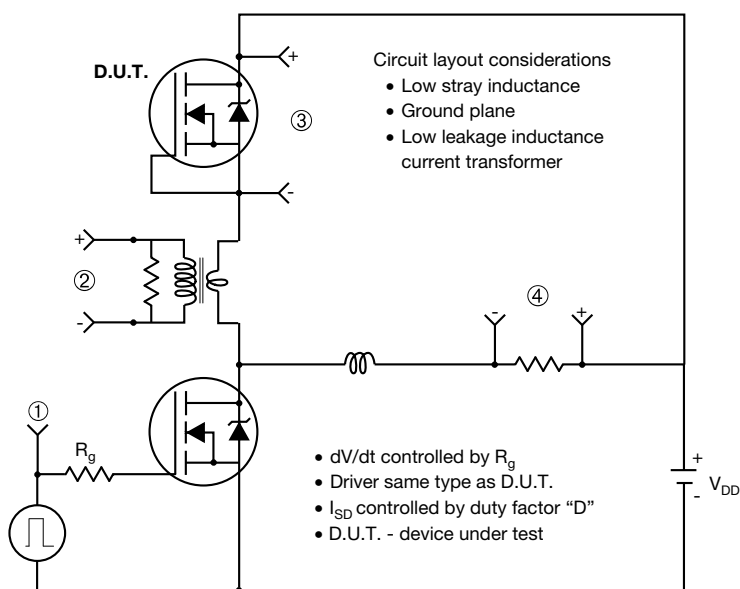


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

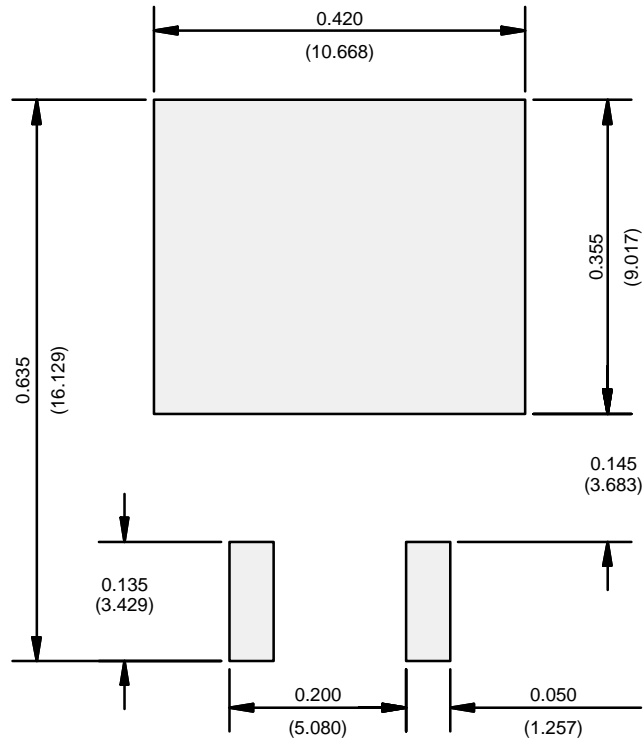


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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