

## IRLR120NTRPBF-VB Datasheet N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
100	0.114 at V <sub>GS</sub> = 10 V	15

### FEATURES

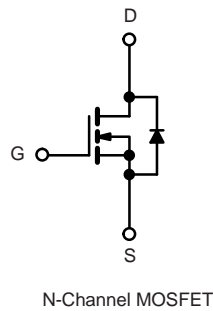
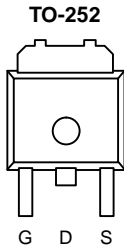
- TrenchFET<sup>®</sup> Power MOSFET
- 150 °C Junction Temperature
- PWM Optimized
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT

### APPLICATIONS

- Primary Side Switch



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	100	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	15	A
	T <sub>C</sub> = 125 °C		13	
Pulsed Drain Current		I <sub>DM</sub>	40	
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	3	
Avalanche Current		I <sub>AS</sub>	3	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	18	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	96 <sup>b</sup>	W
	T <sub>A</sub> = 25 °C		3 <sup>a</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>a</sup>	t ≤ 10 s	R <sub>thJA</sub>	15	18	°C/W
	Steady State		40	50	
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.85	1.1	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

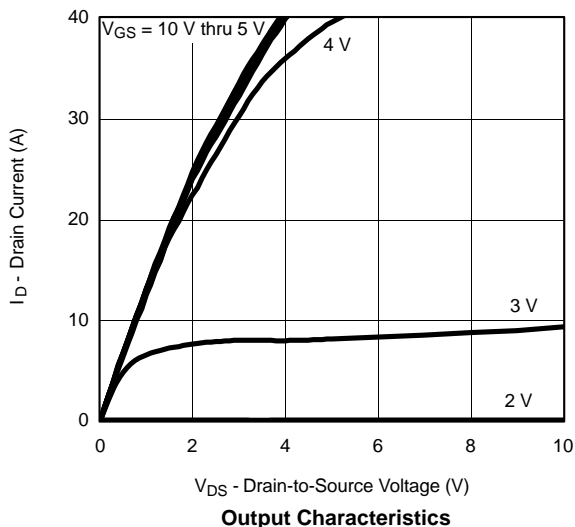
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.114		$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 3\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.120		
		$V_{GS} = 10\text{ V}, I_D = 3\text{ A}, T_J = 175\text{ }^\circ\text{C}$		0.140		
		$V_{GS} = 4.5\text{ V}, I_D = 3\text{ A}$		0.120		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 3\text{ A}$		35		S
<b>Dynamic<sup>a</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, F = 1\text{ MHz}$		950		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			60		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		24	41	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			8		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			12		
Gate Resistance	$R_g$		0.5		2.9	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 5.2\text{ }\Omega$ $I_D \cong 3\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			50	75	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			30	45	
Fall Time <sup>c</sup>	$t_f$			60	90	
<b>Source-Drain Diode Ratings and Characteristics</b> ( $T_C = 25\text{ }^\circ\text{C}$ )						
Pulsed Current	$I_{SM}$				5	A
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 3\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.5	V
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		180	250	ns

Notes:

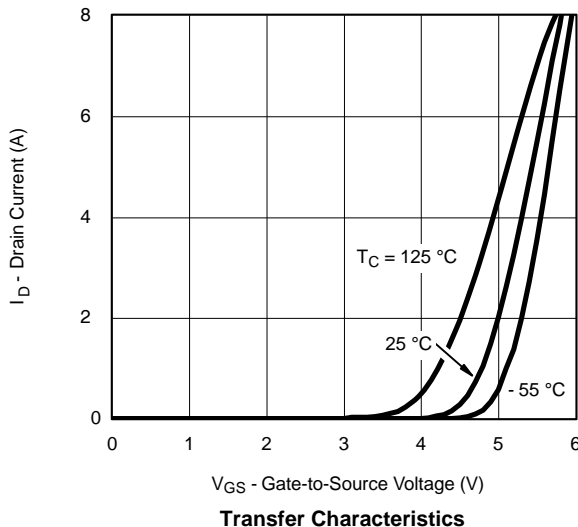
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

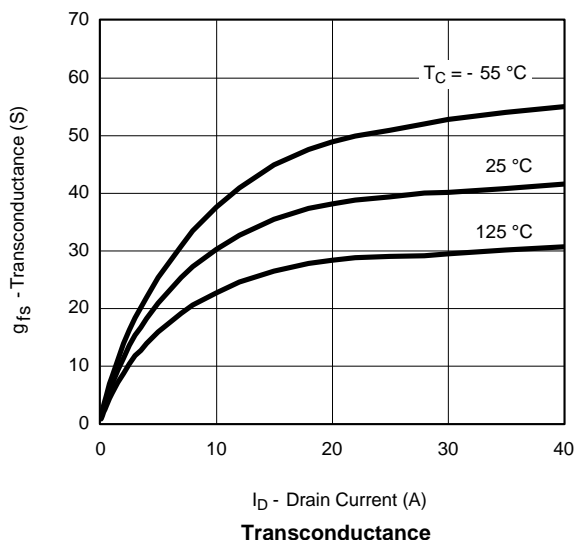
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



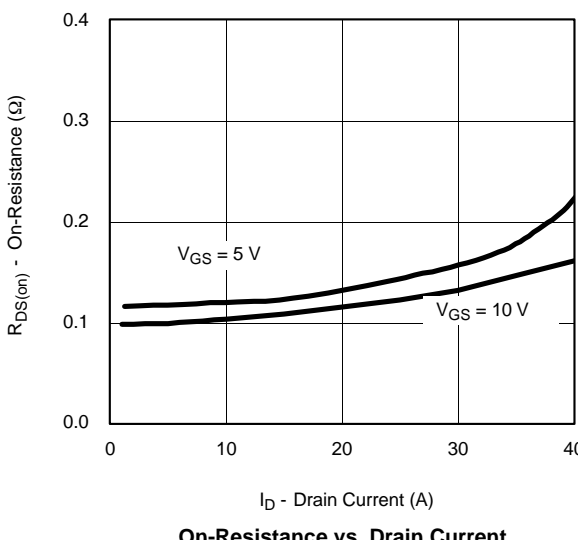
**Output Characteristics**



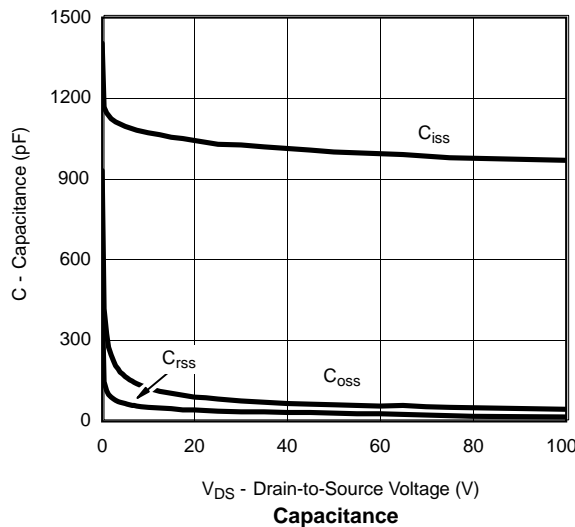
**Transfer Characteristics**



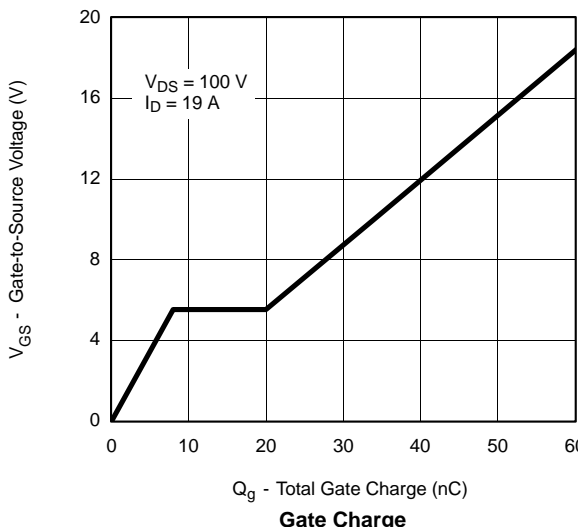
**Transconductance**



**On-Resistance vs. Drain Current**



**Capacitance**

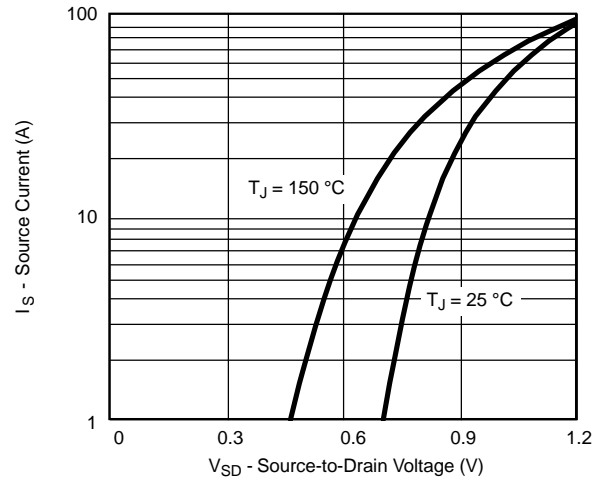


**Gate Charge**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

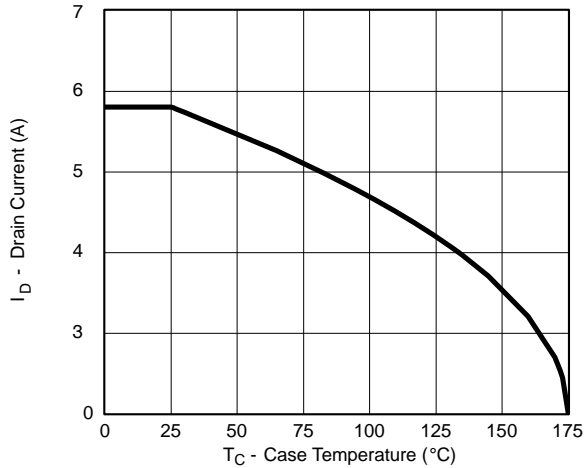


On-Resistance vs. Junction Temperature

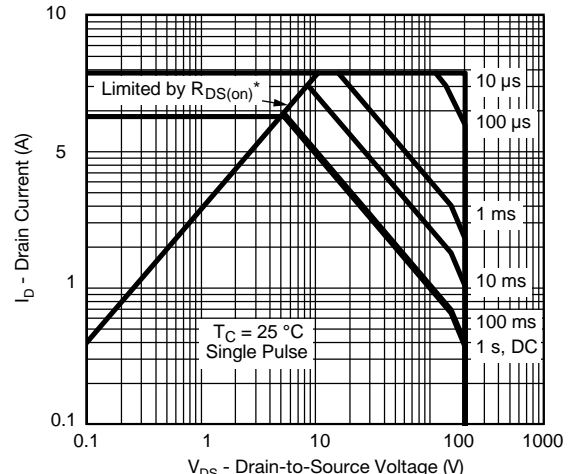


Source-Drain Diode Forward Voltage

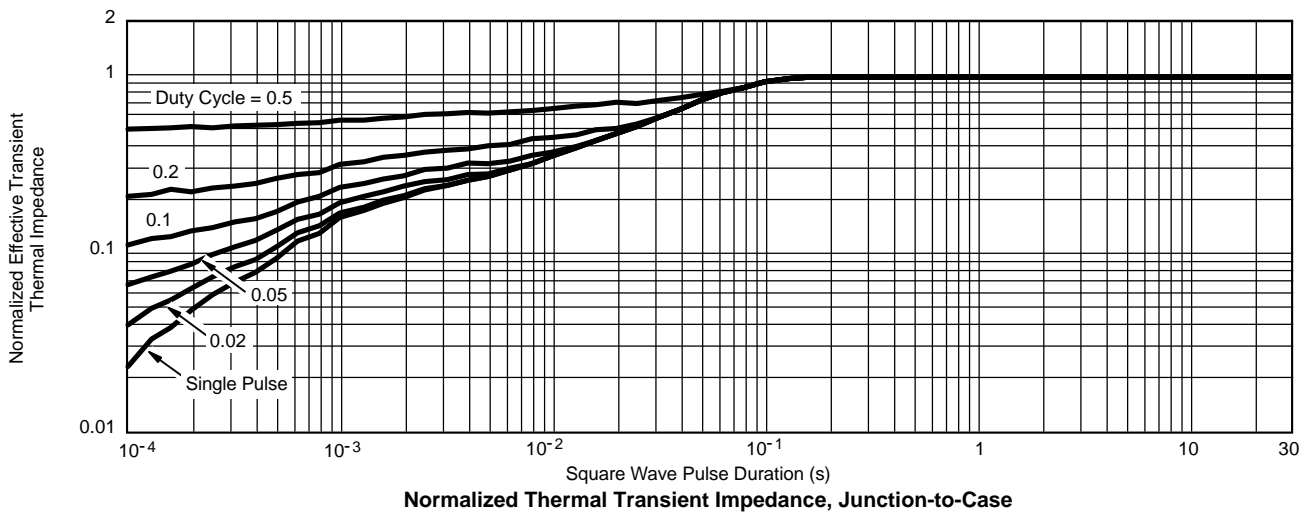
**THERMAL RATINGS**



Maximum Avalanche Drain Current vs. Case Temperature

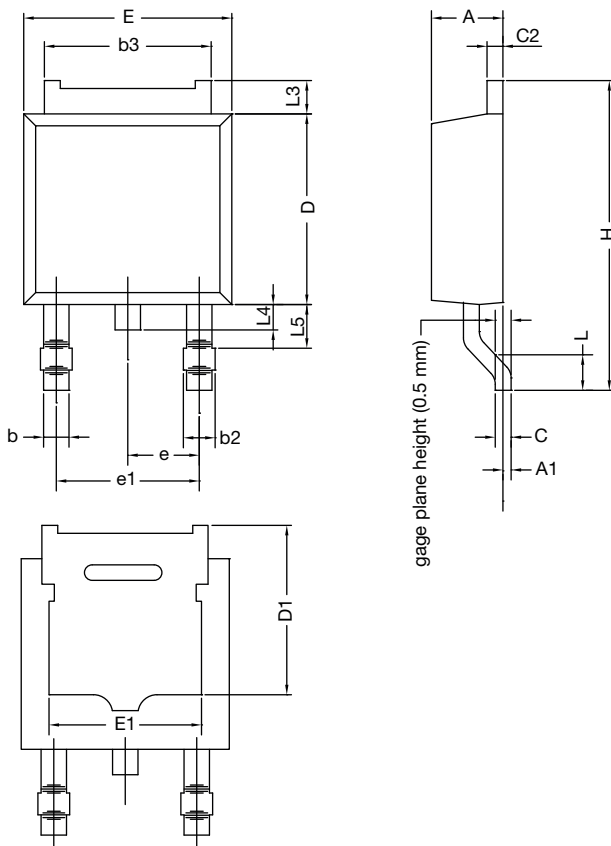


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

## TO-252AA CASE OUTLINE

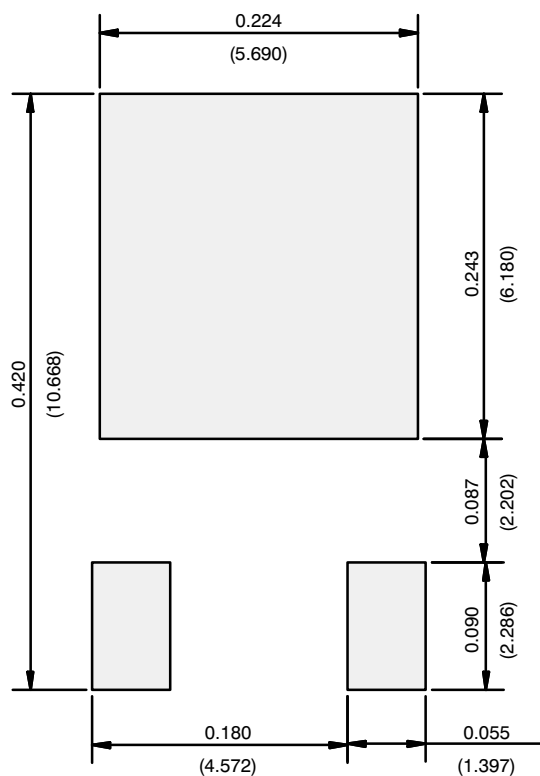


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

**Note**

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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