

## FDD8424H-VB Datasheet

### N- and P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
$V_{DS}$ (V)	40	- 40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = \pm 10$ V	0.014	0.014
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = \pm 4.5$ V	0.016	0.016
$I_D$ (A)	50	- 50
Configuration	N- and P-Pair	

#### FEATURES

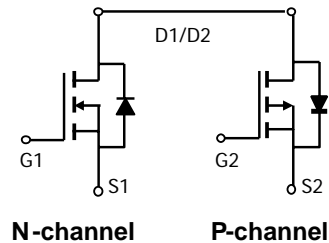
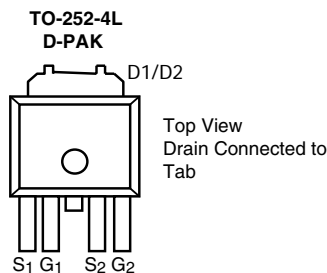
- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

#### APPLICATIONS

- CCFL Inverter



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Drain-Source Voltage	$V_{DS}$	40	- 40	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current <sup>a</sup>	$I_D$	$T_C = 25$ °C	50	-50	A
		$T_C = 125$ °C	35	-35	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	50	-50		
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	150	-150		
Single Pulse Avalanche Current	$I_{AS}$	L = 0.1 mH	30	- 30	mJ
Single Pulse Avalanche Energy			$E_{AS}$	245	
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	108	108	W
		$T_C = 125$ °C	32	32	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175		°C	
Soldering Recommendations (Peak Temperature)		260			

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-Ambient	$R_{thJA}$	85	85	°C/W
Junction-to-Case (Drain)				

#### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.

SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		N-Ch	40	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA		P-Ch	- 40	-	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		N-Ch	1.0	-	3.0	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA		P-Ch	- 1.0	-	-3.0	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	N-Ch	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V	P-Ch	-	-	- 1	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	N-Ch	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V, T <sub>J</sub> = 125 °C	P-Ch	-	-	- 50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	N-Ch	-	-	150	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 40 V, T <sub>J</sub> = 175 °C	P-Ch	-	-	- 150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	N-Ch	25	-	-	A
		V <sub>GS</sub> = - 10 V	V <sub>DS</sub> ≤ 5 V	P-Ch	- 25	-	-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 38 A	N-Ch	-	0.014	-	Ω
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 38 A	P-Ch	-	0.014	-	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 38 A, T <sub>J</sub> = 125 °C	N-Ch	-	0.017	-	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 38 A, T <sub>J</sub> = 125 °C	P-Ch	-	0.017	-	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 38 A, T <sub>J</sub> = 175 °C	N-Ch	-	0.025	-	
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 38 A, T <sub>J</sub> = 175 °C	P-Ch	-	0.025	-	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 30 A	N-Ch	-	0.016	-	
V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 30A	P-Ch	-	0.016	-			
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 38 A		N-Ch	-	40	-	S
		V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 38 A		P-Ch	-	18	-	
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, f = 1 MHz	N-Ch	-	1799	2248	pF
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 20 V, f = 1 MHz	P-Ch	-	2000	3500	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, f = 1 MHz	N-Ch	-	282	352	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 20 V, f = 1 MHz	P-Ch	-	320	550	
Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 20 V, f = 1 MHz	N-Ch	-	109	136	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 20 V, f = 1 MHz	P-Ch	-	220	360	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 A	N-Ch	-	310	-	nC
		V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 20 V, I <sub>D</sub> = - 10 A	P-Ch	-	420	-	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 A	N-Ch	-	5.7	-	
		V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 20 V, I <sub>D</sub> = - 10 A	P-Ch	-	5.5	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 10 A	N-Ch	-	4.8	-	
		V <sub>GS</sub> = - 10 V	V <sub>DS</sub> = - 20 V, I <sub>D</sub> = - 10 A	P-Ch	-	10.5	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		N-Ch	2	4.11	6.2	Ω
				P-Ch	3.1	6.3	9.5	

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

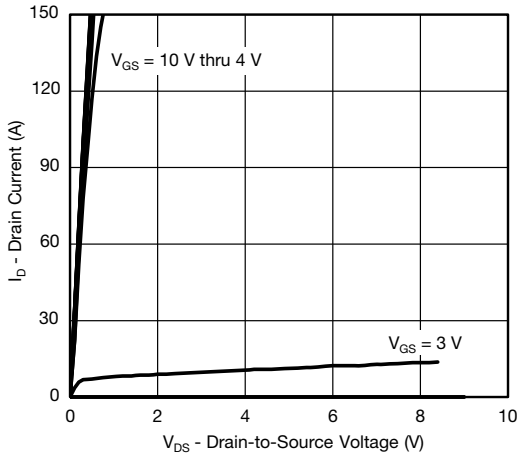
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	7	11	ns
		V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	11	17	
Rise Time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	21	32	
		V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	9	14	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	33	50	
		V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	55	83	
Fall Time <sup>c</sup>	t <sub>f</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	N-Ch	-	19	29	
		V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω	P-Ch	-	91	137	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>		N-Ch	-	-	32	A
			P-Ch	-	-	- 32	
Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4 A	N-Ch	-	0.79	1.2	V
		I <sub>S</sub> = - 4 A	P-Ch	-	- 0.82	- 1.2	

**Notes**

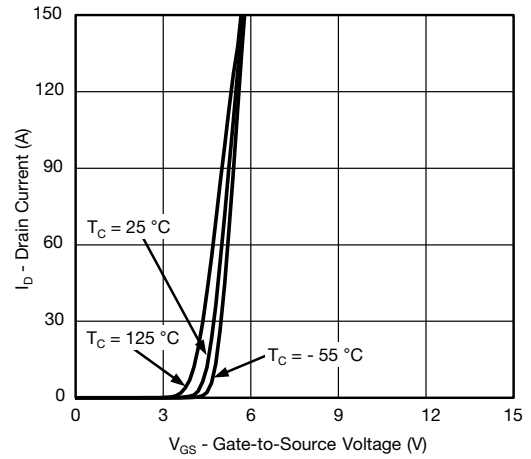
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

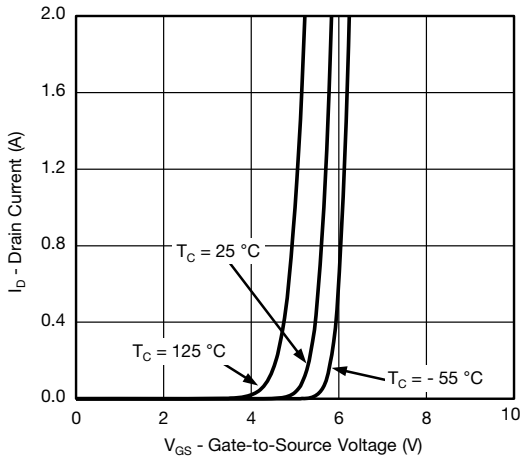
**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



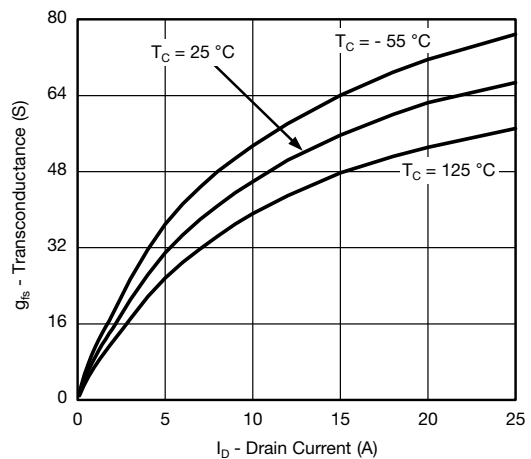
**Output Characteristics**



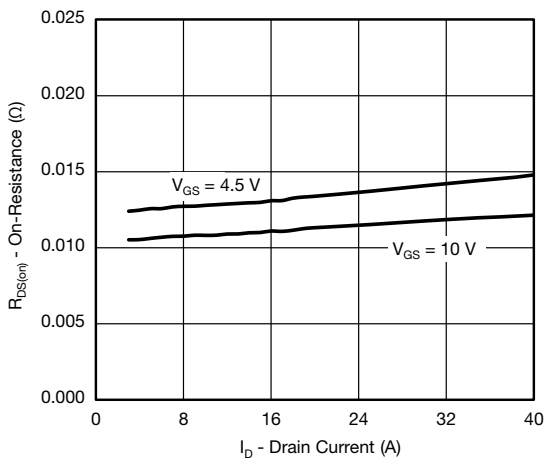
**Transfer Characteristics**



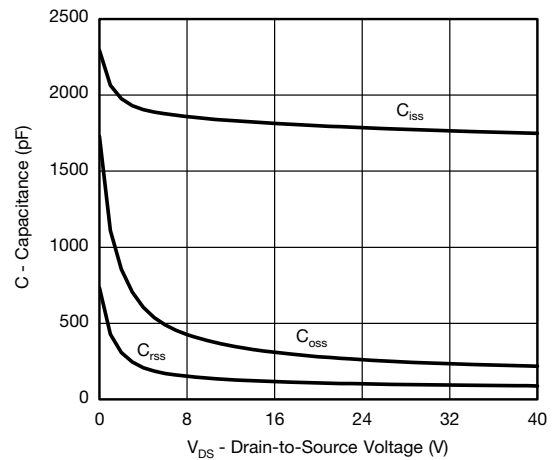
**Transfer Characteristics**



**Transconductance**

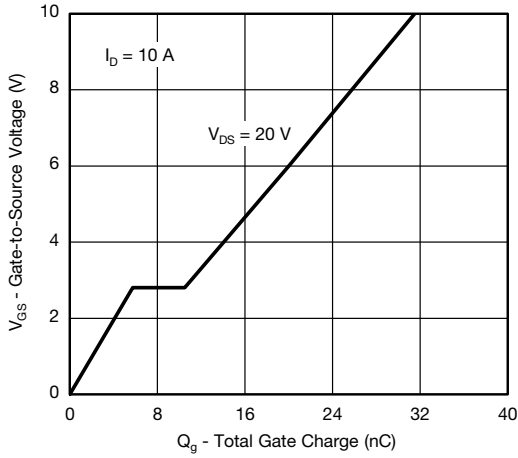


**On-Resistance vs. Drain Current**

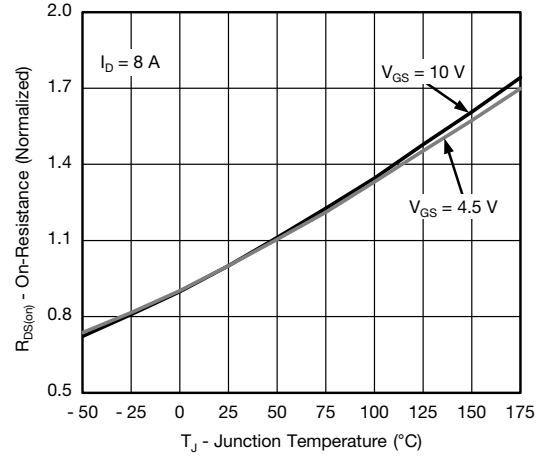


**Capacitance**

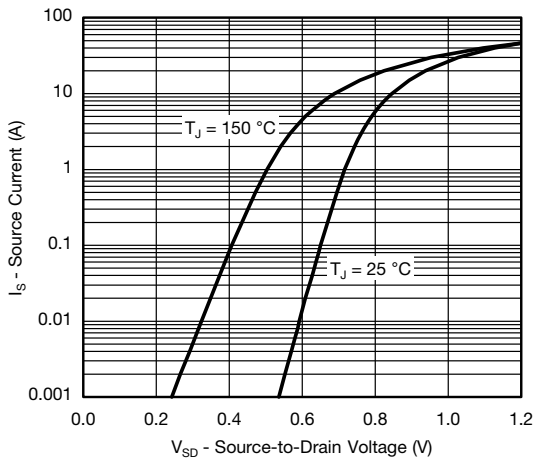
**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



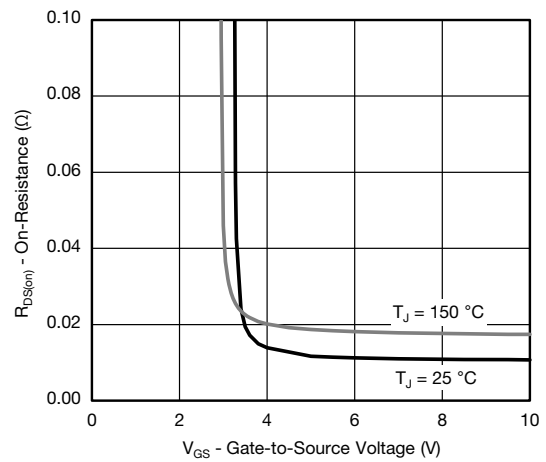
**Gate Charge**



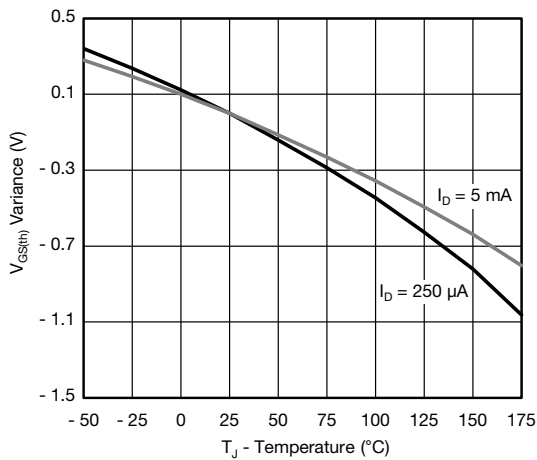
**On-Resistance vs. Junction Temperature**



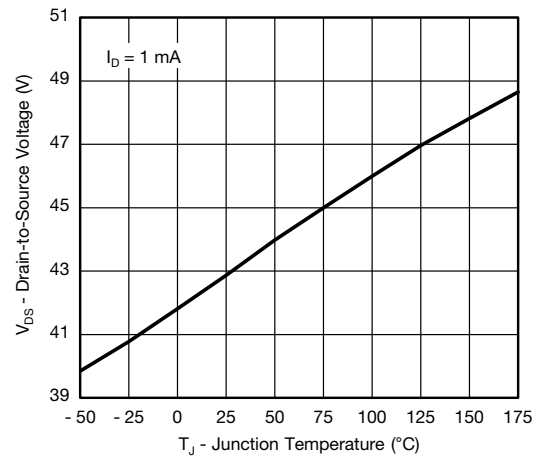
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

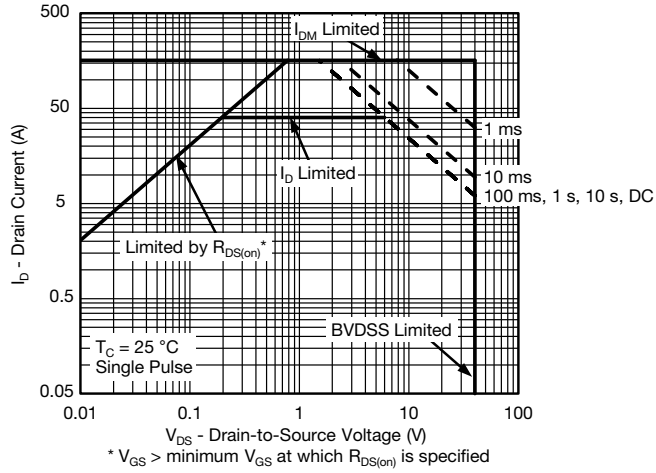


**Threshold Voltage**

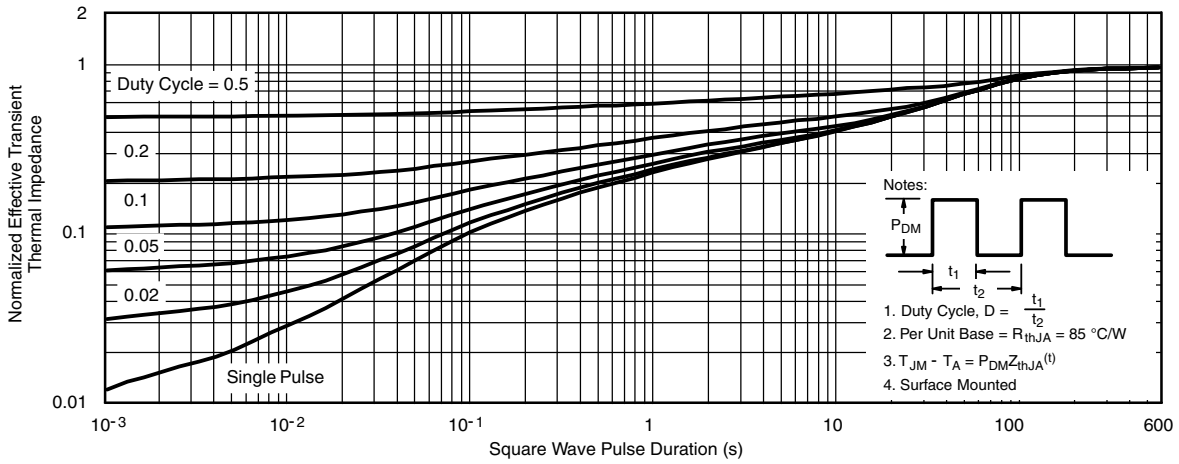


**Drain Source Breakdown vs. Junction Temperature**

**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

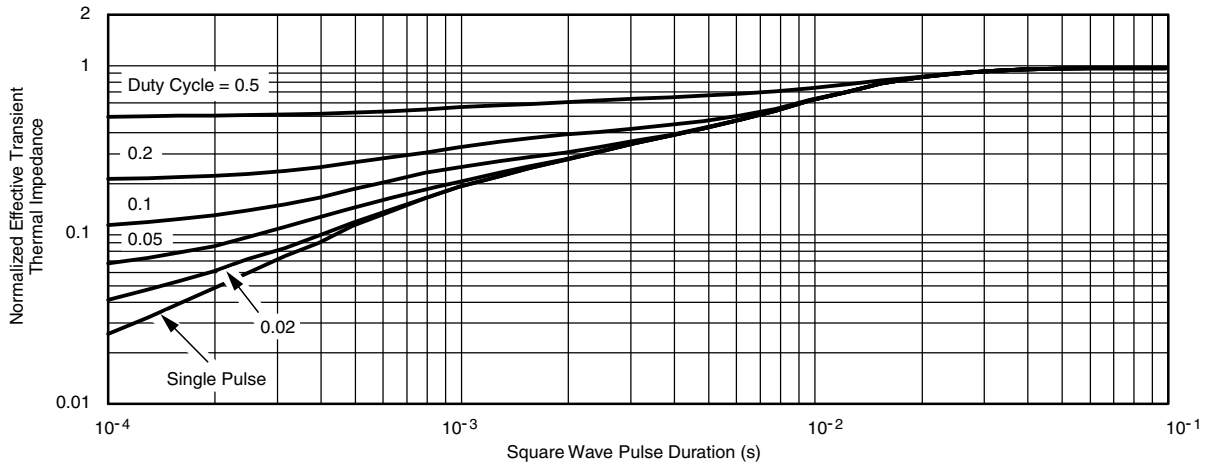


**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**N-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

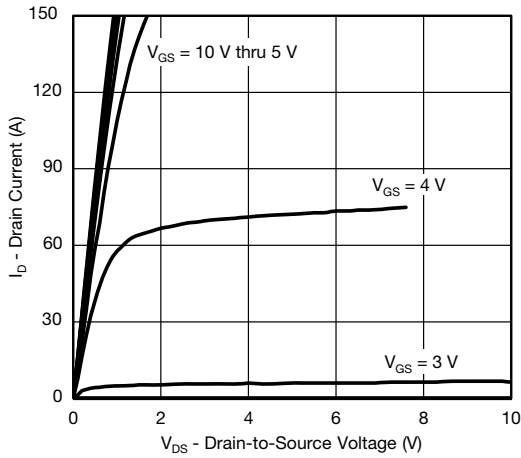


**Normalized Thermal Transient Impedance, Junction-to-Case**

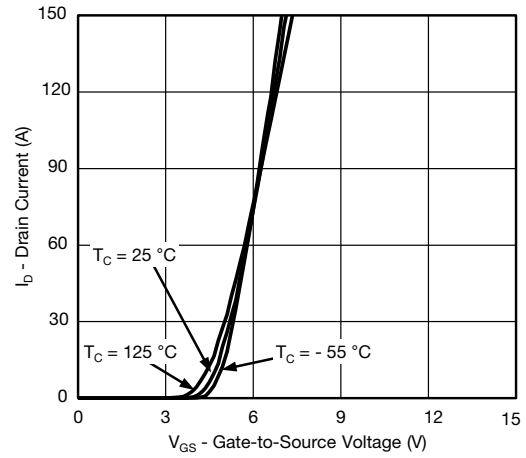
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

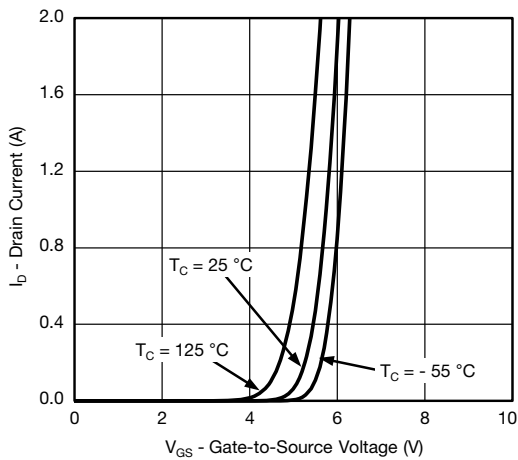
**P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



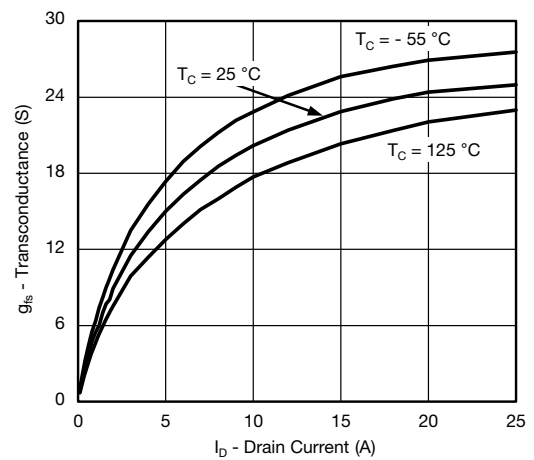
**Output Characteristics**



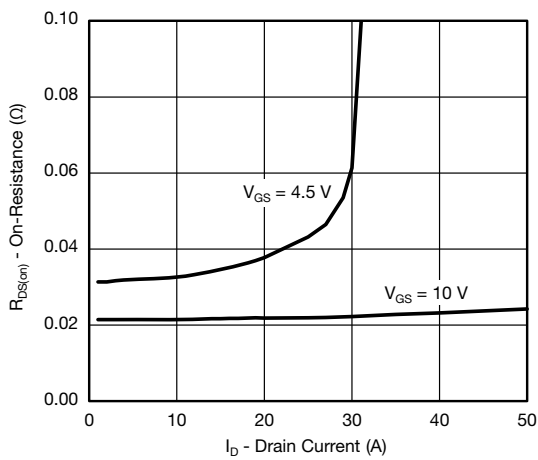
**Transfer Characteristics**



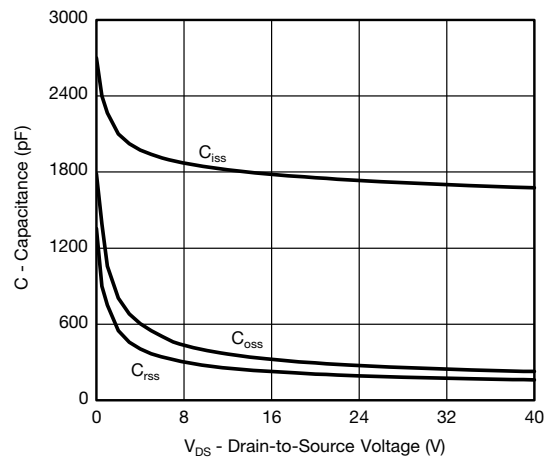
**Transfer Characteristics**



**Transconductance**



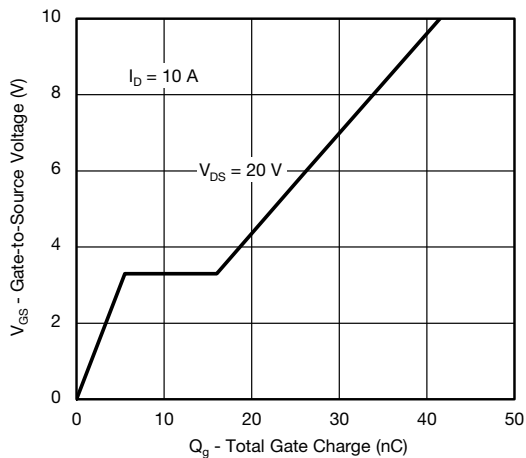
**On-Resistance vs. Drain Current**



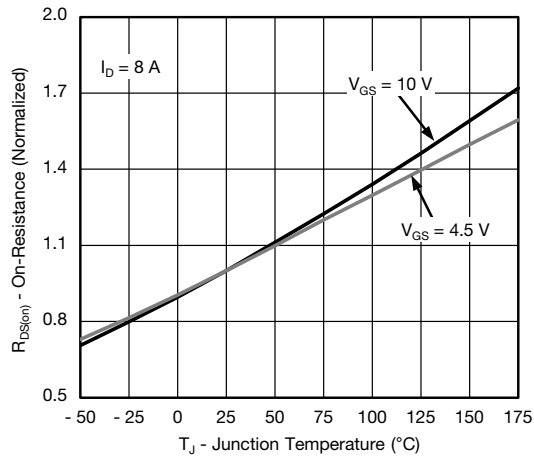
**Capacitance**



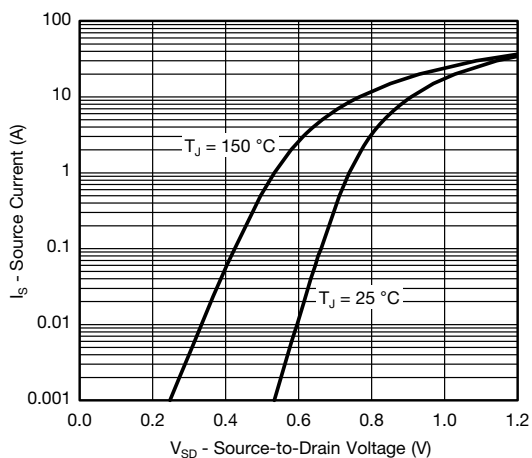
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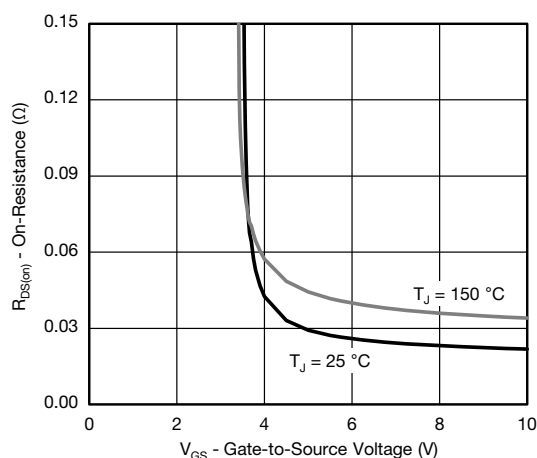
**Gate Charge**



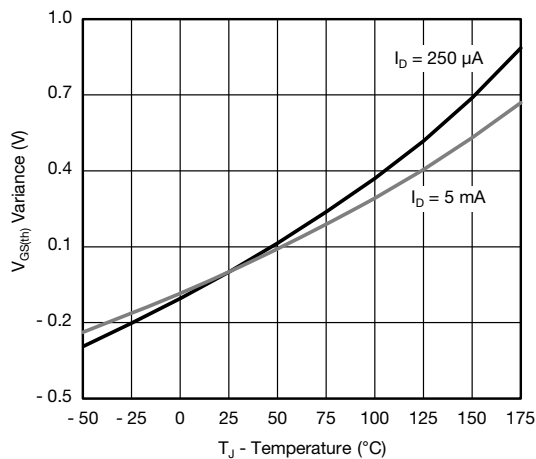
**On-Resistance vs. Junction Temperature**



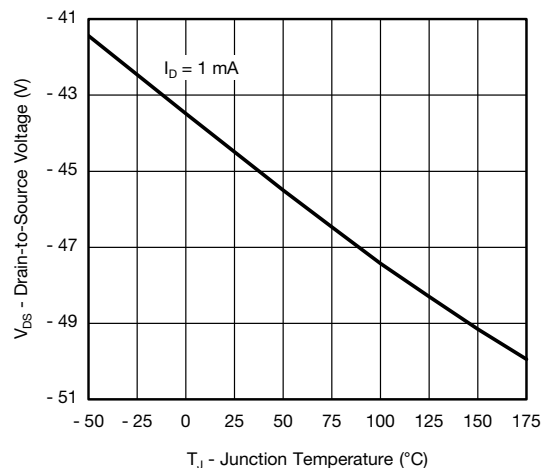
**Source Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

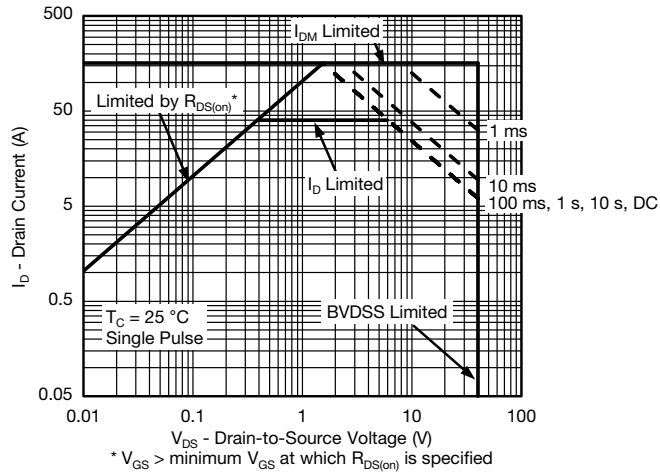


**Threshold Voltage**

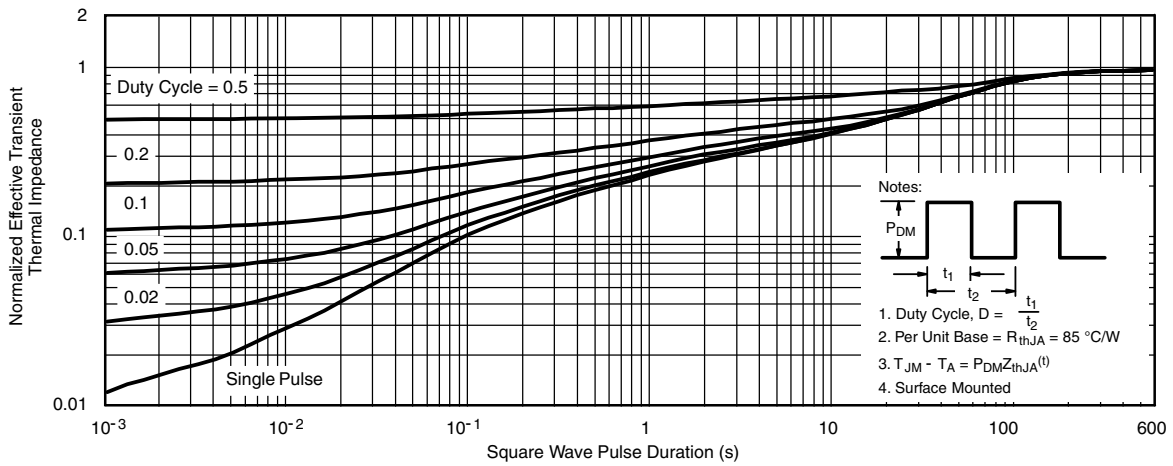


**Drain Source Breakdown vs. Junction Temperature**

**P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

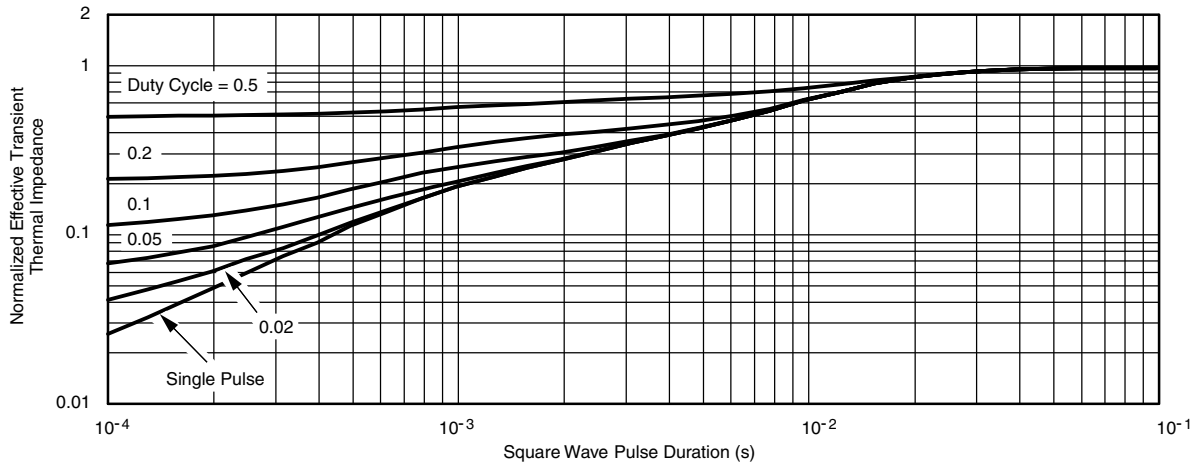


**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**P-CHANNEL TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

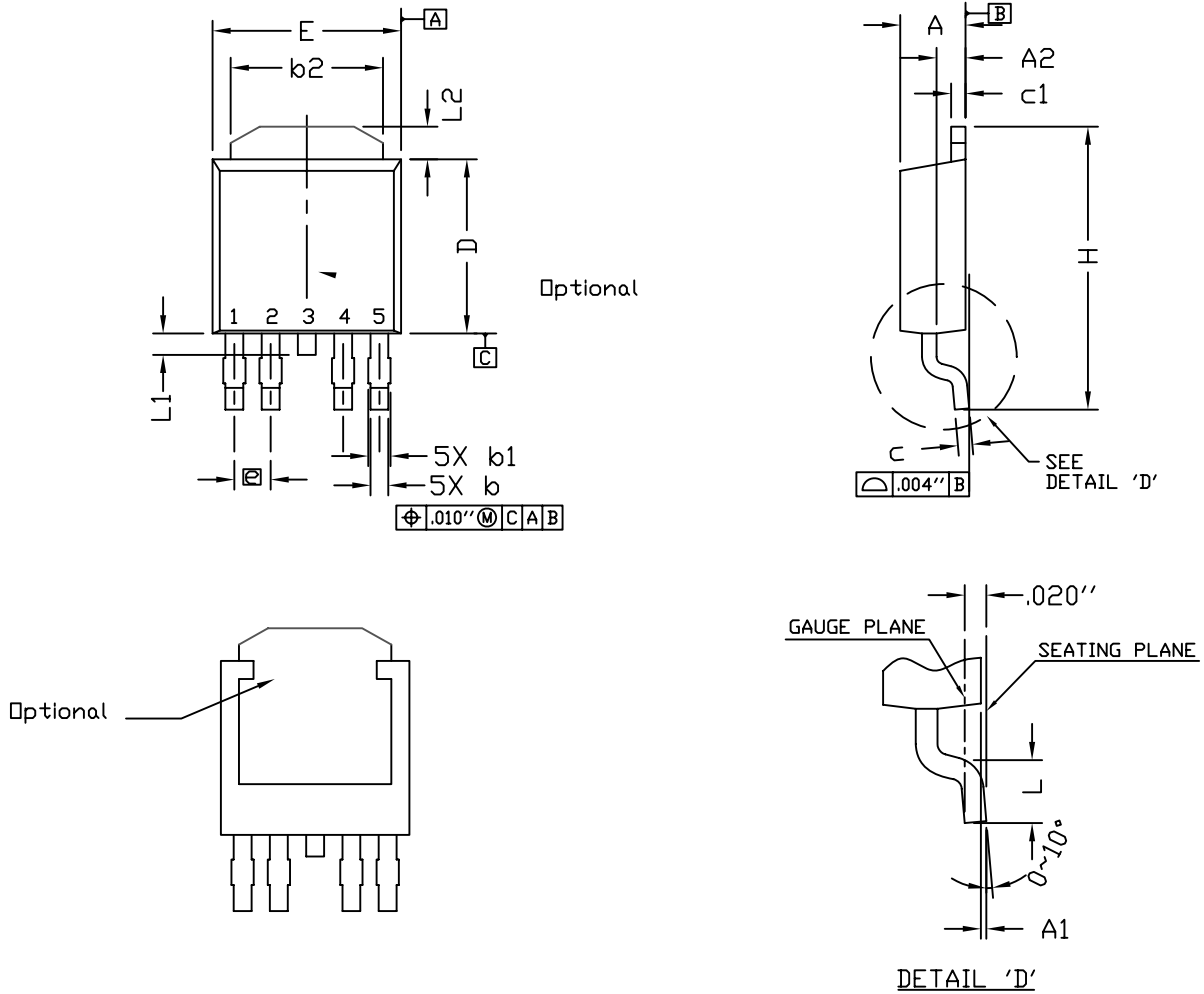


**Normalized Thermal Transient Impedance, Junction-to-Case**

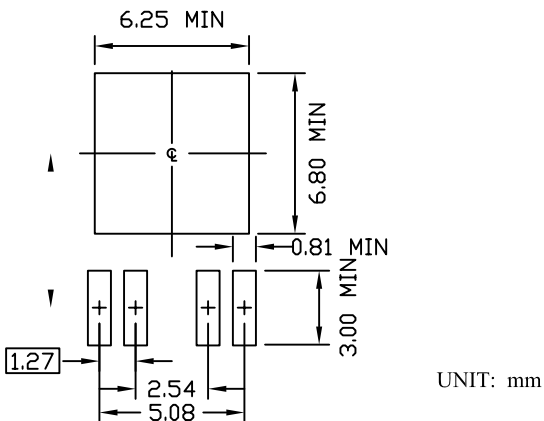
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

### TO-252\_4L Package Outline



#### RECOMMENDED LAND PATTERN



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	----	0.127	0.000	----	0.005
A2	0.889	----	1.143	0.035	----	0.045
b	0.508	----	0.711	0.020	----	0.028
b1	0.584	----	0.787	0.023	----	0.031
b2	4.953	----	5.461	0.195	----	0.215
c	0.457	0.508	0.610	0.018	0.020	0.024
c1	0.457	----	0.610	0.018	----	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
E	6.350	6.604	6.731	0.250	0.260	0.265
e	1.270 BSC.			0.050 BSC.		
H	9.398	----	10.414	0.370	----	0.410
L	1.270	----	2.032	0.050	----	0.080
L1	----	----	1.016	----	----	0.040
L2	0.889	----	1.270	0.035	----	0.050

- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
  2. DIMENSION L IS MEASURED IN GAUGE PLANE.
  3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
  4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
  5. REFER TO JEDEC TO-252 (AD).

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**Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.**

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