

# STP32NM50N-VB Datasheet

## N-Channel 500-V (D-S) Super Junction MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V) at $T_J$ max.	500	
$R_{DS(on)}$ at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.115
$Q_g$ (Max.) (nC)	86	
$Q_{gs}$ (nC)	14	
$Q_{gd}$ (nC)	25	
Configuration	Single	

### FEATURES

- Low figure-of-merit (FOM):  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)

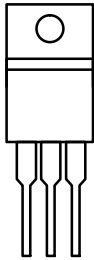


RoHS  
COMPLIANT  
HALOGEN  
FREE

### APPLICATIONS

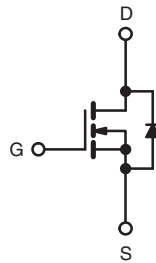
- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
  - PC silver box / ATX power supplies
- Computing
  - Two stage LED lighting

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G D S

Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		500	V
Gate-Source Voltage	$V_{GS}$		$\pm 30$	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	30	A
		$T_C = 100$ °C	18	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		105	
Linear Derating Factor			0.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		273	mJ
Maximum Power Dissipation	$P_D$		280	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		-55 to +150	°C
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % $V_{DS}$		65	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>			25	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s		300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 4.4$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.

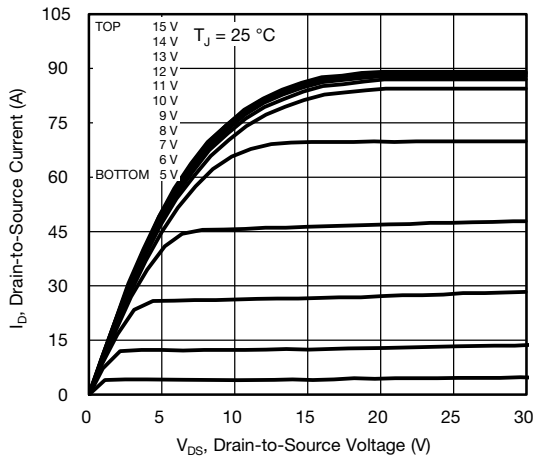
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.5	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.59	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V	-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	1	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	25	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A	-	0.115	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 12 A	-	6.6	-	S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz	-	1980	-	pF
Output Capacitance	C <sub>oss</sub>		-	105	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	8	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>		-	105	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	285	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A, V <sub>DS</sub> = 400 V	-	57	86	nC
Gate-Source Charge	Q <sub>gs</sub>		-	14	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	25	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 12 A R <sub>g</sub> = 9.1 Ω, V <sub>GS</sub> = 10 V	-	19	38	ns
Rise Time	t <sub>r</sub>		-	36	72	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	57	86	
Fall Time	t <sub>f</sub>		-	29	58	
Gate Input Resistance	R <sub>g</sub>		f = 1 MHz, open drain	-	0.56	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	12	A
Pulsed Diode Forward Current	I <sub>SM</sub>		-	-	50	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 16.5 A, V <sub>GS</sub> = 0 V	-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , dI/dt = 100 A/μs, V <sub>R</sub> = 25 V	-	338	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>		-	5.3	-	μC
Reverse Recovery Current	I <sub>RRM</sub>		-	29	-	A

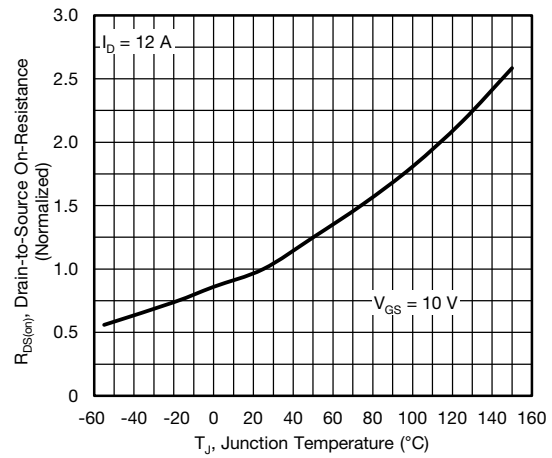
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>.

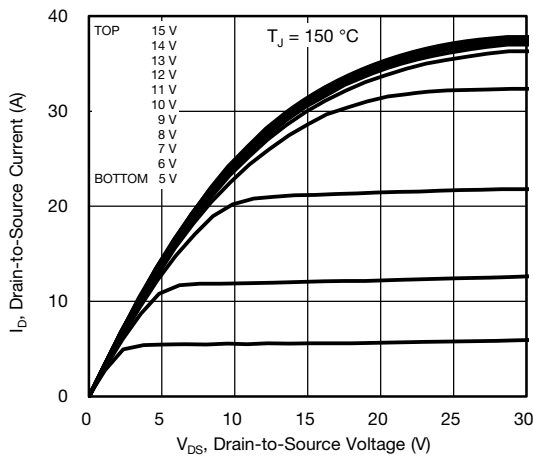
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



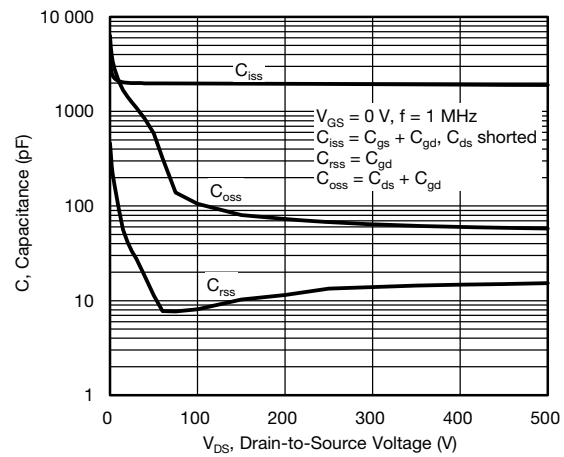
**Fig. 1 - Typical Output Characteristics**



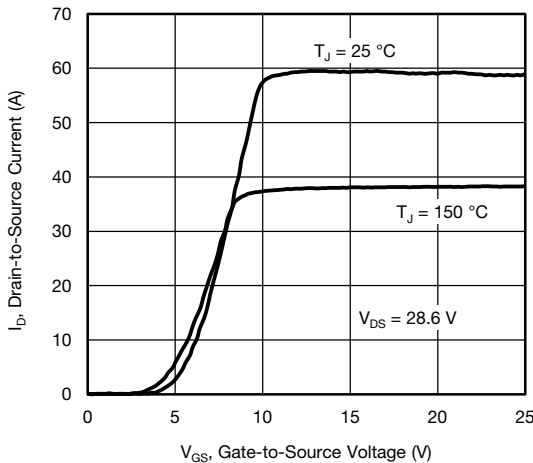
**Fig. 4 - Normalized On-Resistance vs. Temperature**



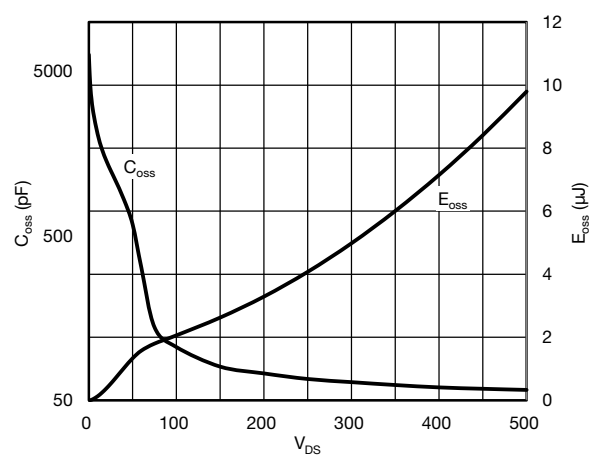
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Coss and Eoss vs. VDS**

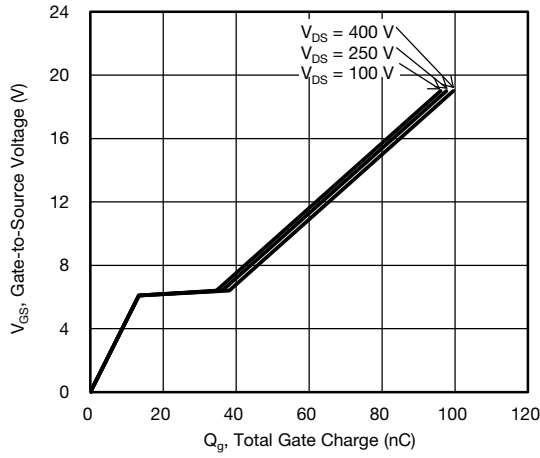


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

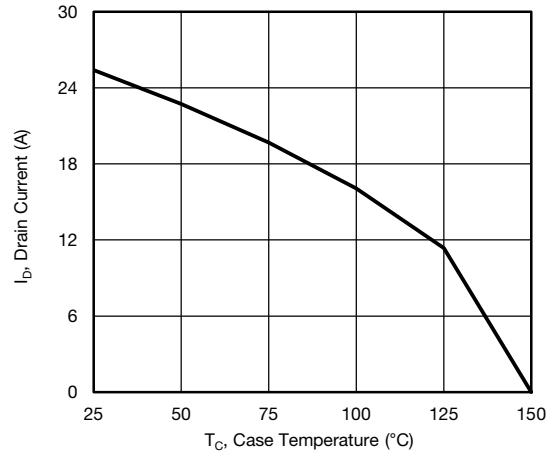


Fig. 10 - Maximum Drain Current vs. Case Temperature

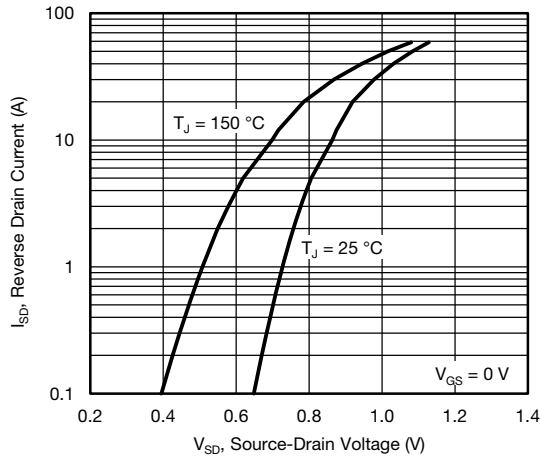


Fig. 8 - Typical Source-Drain Diode Forward Voltage

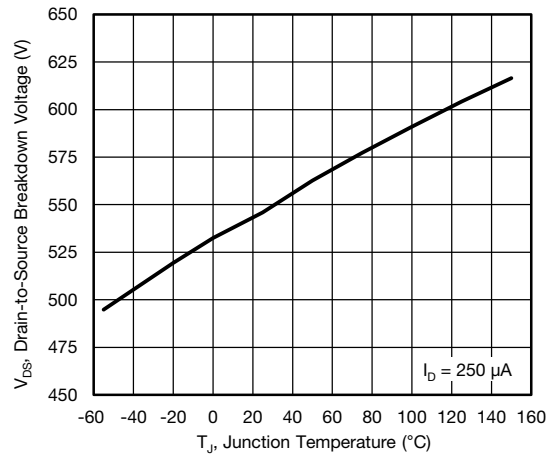


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

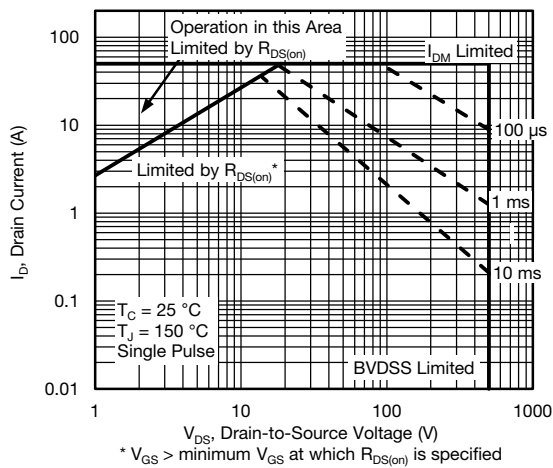


Fig. 9 - Maximum Safe Operating Area

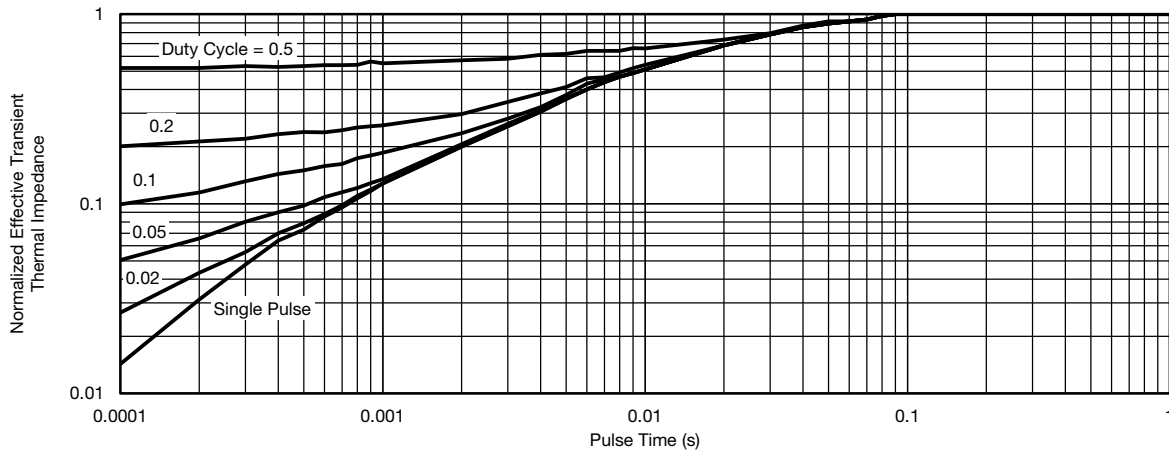


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

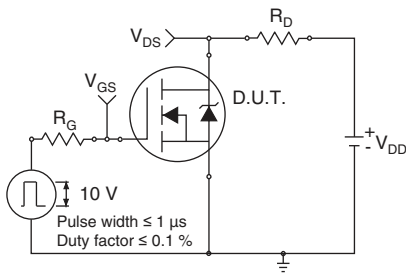


Fig. 13 - Switching Time Test Circuit

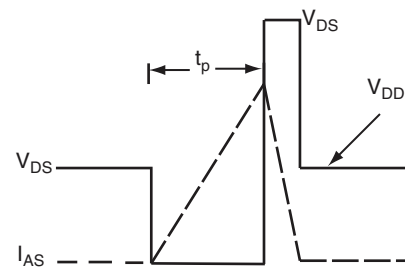


Fig. 16 - Unclamped Inductive Waveforms

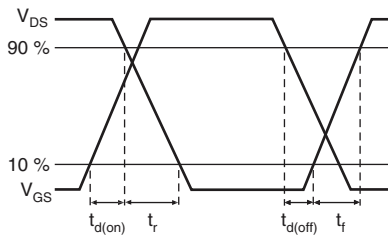


Fig. 14 - Switching Time Waveforms

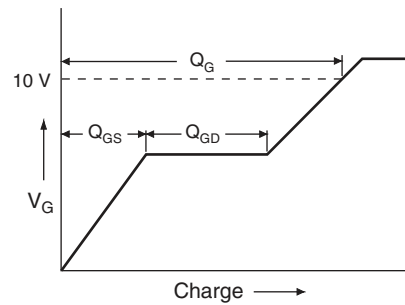


Fig. 17 - Basic Gate Charge Waveform

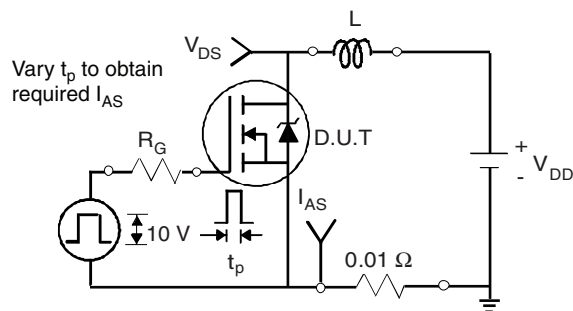


Fig. 15 - Unclamped Inductive Test Circuit

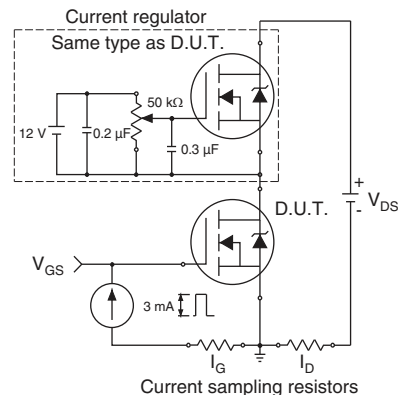
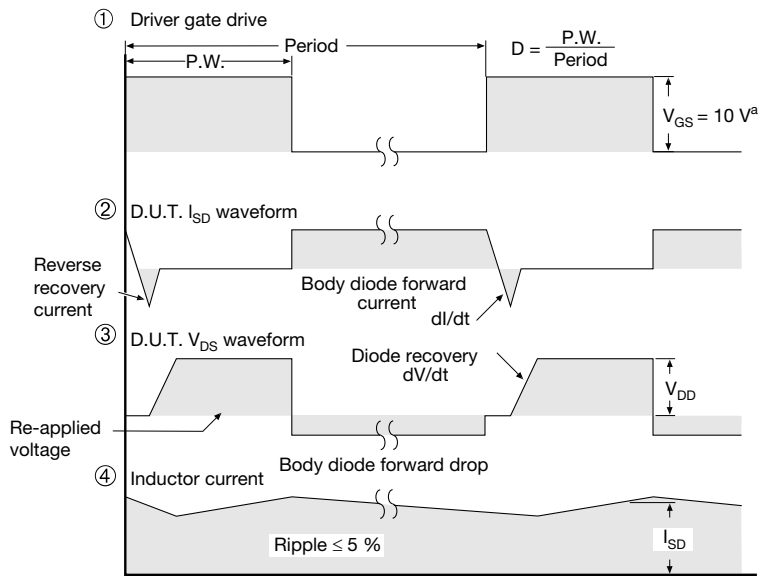
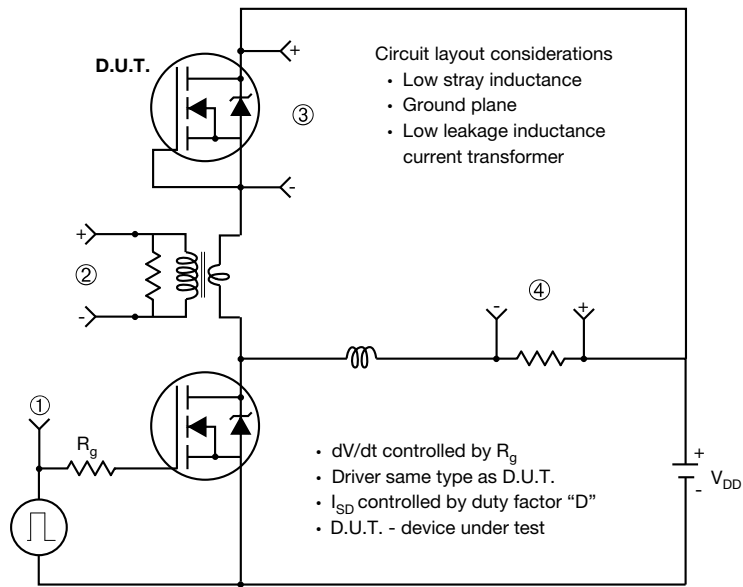


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

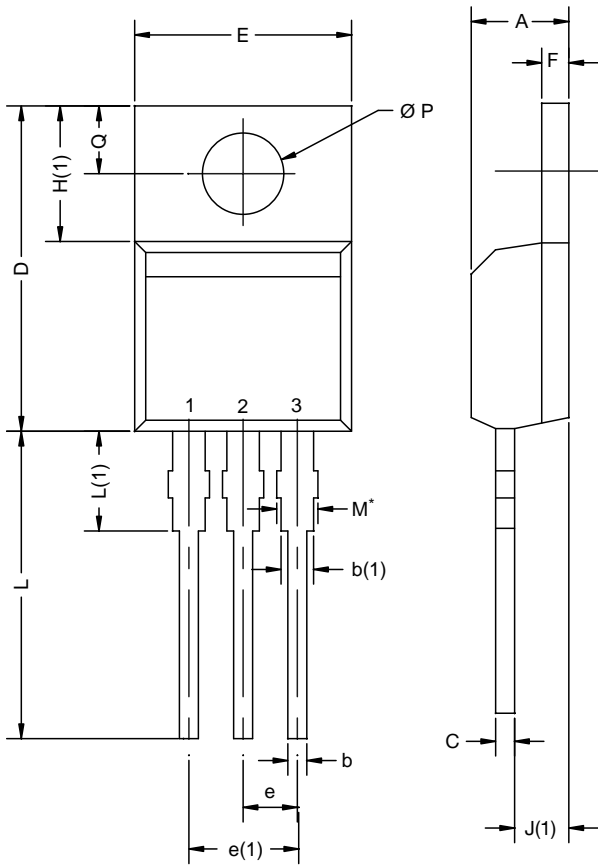


Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM

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