**TO-220AB** 

( )

GDS

Top View



### SPP15N60C3-VB Datasheet

## N-Channel 650 V (D-S) Super Junction MOSFET

PRODUCT SUMMA	RY			
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650			
R <sub>DS(on)</sub> (Ω) at 25 °C	$V_{GS} = 10 V$	0.19		
Q <sub>g</sub> max. (nC)	106			
Q <sub>gs</sub> (nC)	14			
Q <sub>gd</sub> (nC)	33			
Configuration	Sing	le		

GC

S

N-Channel MOSFET

### **FEATURES**

- Reduced t<sub>rr</sub>, Q<sub>rr</sub>, and I<sub>RRM</sub>
- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (Ciss)
- Low switching losses due to reduced Q<sub>rr</sub>
- Ultra low gate charge (Q<sub>a</sub>)
- Avalanche energy rated (UIS)

### **APPLICATIONS**

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power supplies (SMPS)

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> :	= 25 °C, unl	ess otherwis	se noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	650	V	
Gate-Source Voltage		V <sub>GS</sub>	± 30	v	
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25 \ ^{\circ}{\rm C}$ $T_{\rm C} = 100 \ ^{\circ}{\rm C}$	1	20	
Continuous Drain Current (1j = 150°C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	13	A
ulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	60	ĺ	
Linear Derating Factor				1.7	W/°C
Single Pulse Avalanche Energy <sup>b</sup>		E <sub>AS</sub>	367	mJ	
Maximum Power Dissipation		PD	208	W	
Operating Junction and Storage Temperature Range	e		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	Itage Slope $T_J = 125 ^{\circ}C$ $dV/dt$ $37$ $V/ns$		\//no		
Reverse Diode dV/dt d		uv/di	31	v/fis	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	Soldering Recommendations (Peak Temperature) c for 10 s			300	°C

#### Notes

a. Repetitive rating; pulse width limited by maximum junction temperature. b.  $V_{DD} = 50$  V, starting T<sub>J</sub> = 25 °C, L = 28.2 mH, R<sub>g</sub> = 25  $\Omega$ , I<sub>AS</sub> = 5.1 A.

c. 1.6 mm from case.

d.  $I_{SD} \leq I_D$ , dl/dt = 100 A/µs, starting  $T_J$  = 25 °C.



HALOGEN



THERMAL RESISTANCE RATI	NGS							
PARAMETER	SYMBOL	TYP.		MAX.			UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-		62				
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-		0.5		°C/W		
		•						
<b>SPECIFICATIONS</b> ( $T_J = 25 \ ^{\circ}C$ , u	Inless otherw	ise noted)						
PARAMETER	SYMBOL		T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT
Static					1		1	<u> </u>
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> :	= 0 V, I <sub>D</sub> =	250 µA	650	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C	I <sub>D</sub> = 1 mA	-	0.67	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>		= V <sub>GS</sub> , I <sub>D</sub> =		2	-	4	V
			$V_{GS} = \pm 20$	) V	-	-	± 100	nA
Gate-Source Leakage	I <sub>GSS</sub>		$V_{GS} = \pm 30$	) V	-	-	± 1	μA
			= 520 V, V <sub>0</sub>		-	-	1	μA
Zero Gate Voltage Drain Current	IDSS			V, T <sub>J</sub> = 125 °C	-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V		<sub>D</sub> = 11 A	-	0.19	-	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 11 A		-	7.0	-	S	
Dynamic		•			•	•	•	
Input Capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 \	1	-	2322	-	
Output Capacitance	C <sub>oss</sub>		$V_{DS} = 100$		-	105	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		-	4	-	1	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>		(1. 500.)/		-	84	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>	$V_{\rm DS} = 0.0$	/ to 520 V,	$v_{GS} = 0 v$	-	293	-	
Total Gate Charge	Qg				-	71	106	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11	A, V <sub>DS</sub> = 520 V	-	14	-	nC
Gate-Drain Charge	Q <sub>gd</sub>				-	33	-	
Turn-On Delay Time	t <sub>d(on)</sub>		$V_{DD}$ = 520 V, I <sub>D</sub> = 11 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	22	44	
Rise Time	t <sub>r</sub>	V <sub>DD</sub> =			-	34	68	ns
Turn-Off Delay Time	t <sub>d(off)</sub>	V <sub>GS</sub> :			-	68	102	
Fall Time	t <sub>f</sub>	1		-	42	84		
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.78	-	Ω	
Drain-Source Body Diode Characteristi	cs							
Continuous Source-Drain Diode Current	١ <sub>S</sub>	MOSFET sym showing the	bol		-	-	21	
Pulsed Diode Forward Current	I <sub>SM</sub>	integral revers p - n junction			-	-	53	A
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °	C, I <sub>S</sub> = 11 /	A, V <sub>GS</sub> = 0 V	-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>				-	160	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	$T_J = 2$	5 °C, I <sub>F</sub> = I	S = 11 A,	-	1.2	-	μC
Reverse Recovery Current	I <sub>RRM</sub>	ai/at =	100 A/µs,	$v_{\rm R} = 25 V$	-	14	-	A

### Notes

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ . b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

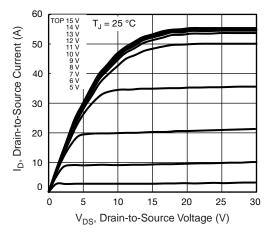


Fig. 1 - Typical Output Characteristics



Fig. 2 - Typical Output Characteristics

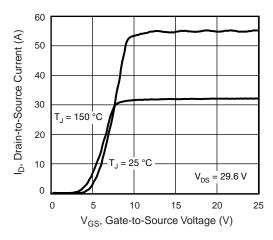


Fig. 3 - Typical Transfer Characteristics

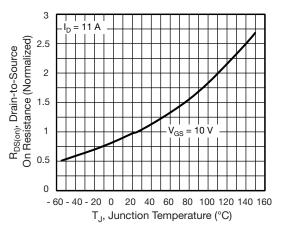


Fig. 4 - Normalized On-Resistance vs. Temperature

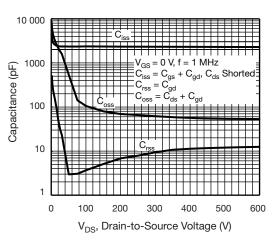


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

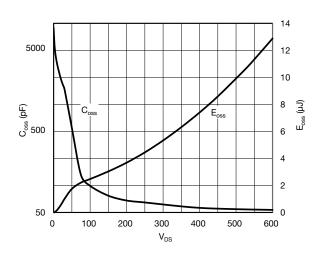


Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$ 

### SPP15N60C3-VB



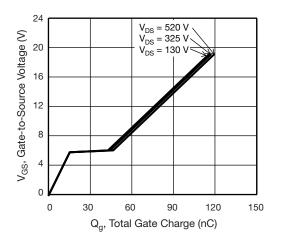


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

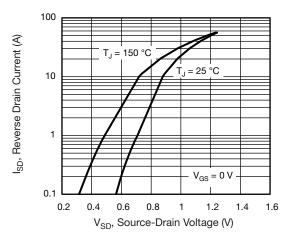


Fig. 8 - Typical Source-Drain Diode Forward Voltage

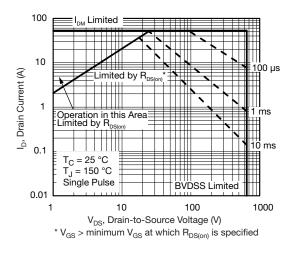


Fig. 9 - Maximum Safe Operating Area

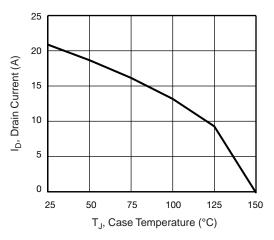


Fig. 10 - Maximum Drain Current vs. Case Temperature



Fig. 11 - Temperature vs. Drain-to-Source Voltage



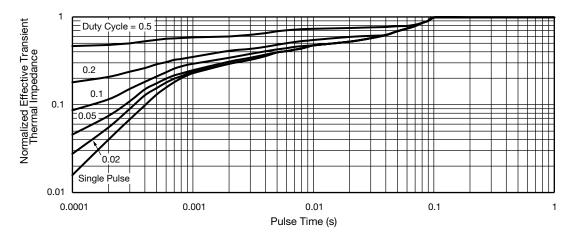


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 14 - Switching Time Waveforms

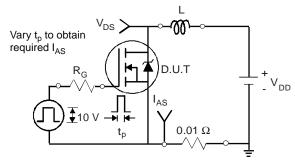


Fig. 15 - Unclamped Inductive Test Circuit

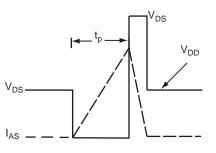


Fig. 16 - Unclamped Inductive Waveforms

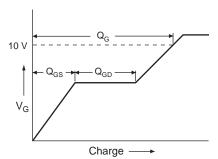
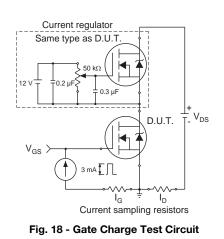
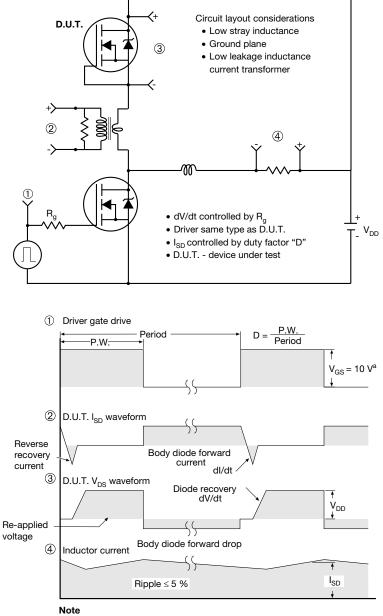


Fig. 17 - Basic Gate Charge Waveform





### Peak Diode Recovery dV/dt Test Circuit

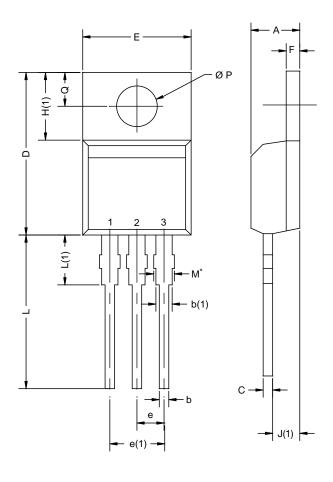


a.  $V_{GS} = 5$  V for logic level devices

Fig. 19 - For N-Channel



# **TO-220AB**



	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	

### Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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