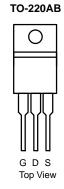


ROHS COMPLIANT

NCE40H25-VB Datasheet

N-Channel 40 V (D-S) MOSFET

PRODU	CT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, c}	Q _g (Typ.)
40	0.0010 at V _{GS} = 10 V	280	240 nC
40	0.0012 at V_{GS} = 4.5 V	250	240110

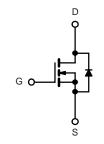


FEATURES

- TrenchFET[®] Power MOSFET
- 100 % $\rm R_g$ and UIS Tested

APPLICATIONS

- Synchronous Rectification
- Power Supplies



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unle	ss otherwise n	oted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	40	V
Gate-Source Voltage		V _{GS}	± 25	v
	T _C = 25 °C		280 ^{a, c}	
Continuous Drain Current (T 175 °C)	T _C = 70 °C		220 ^c	
Continuous Drain Current ($T_J = 175 \ ^{\circ}C$)	T _A = 25 °C	. I _D	229 ^b	A
	T _A = 70 °C		223 ^b	
Pulsed Drain Current		I _{DM}	750	
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	80	
Single Pulse Avalanche Energy	L = 0.1 IIIH	E _{AS}	320	V
Continuous Source-Drain Diode Current	T _C = 25 °C	la	110 ^{a, c}	A
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.6 ^b	
	T _C = 25 °C		312 ^a	
Maximum Power Dissipation	T _C = 70 °C	PD	200	w
	T _A = 25 °C		3.13 ^b	vv
	T _A = 70 °C		2.0 ^b	7
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	32	40	°C/W
Maximum Junction-to-Case	Steady State	R _{thJC}	0.33	0.4	0,00

Notes:

a. Based on $T_C = 25 \ ^{\circ}C$.

b. Surface Mounted on 1" x 1" FR4 board.

c. Calculated based on maximum junction temperature. Package limitation current is 110 A.

SPECIFICATIONS $T_J = 25 \text{ °C}, $	unless other	wise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	45			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		41		m\//ºC	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	iβ = 200 μΛ		- 8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	цА	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			A	
	D	V _{GS} = 10 V, I _D = 30 A		0.0010		0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0012		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A		180		S	
Dynamic ^b	1					I	
Input Capacitance	C _{iss}			18800		V mV/°C V nA μA A	
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$		1550			
Reverse Transfer Capacitance	C _{rss}			850			
Total Gate Charge	Qg			240	360		
Gate-Source Charge	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$		40		nC	
Gate-Drain Charge	Q _{gd}			22			
Gate Resistance	R _g	f = 1 MHz		0.85	1.3	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	V_{DD} = 20 V, R_{L} = 1.0 Ω		11	17		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		77	115		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			102	155	ns	
Rise Time	t _r	V_{DD} = 20 V, R_L = 1.0 Ω		62	95	-	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 20 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		180	270		
Fall Time	t _f	-		60	90		
Drain-Source Body Diode Characteristic						<u> </u>	
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			110	_	
Pulse Diode Forward Current ^a	I _{SM}				200		
Body Diode Voltage	V _{SD}	I _S = 20 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			50	75	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			70	105	nC	
Reverse Recovery Fall Time	t _a	$I_F = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^\circ\text{C}$		30			
Reverse Recovery Rise Time	t _b			20		ns	

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

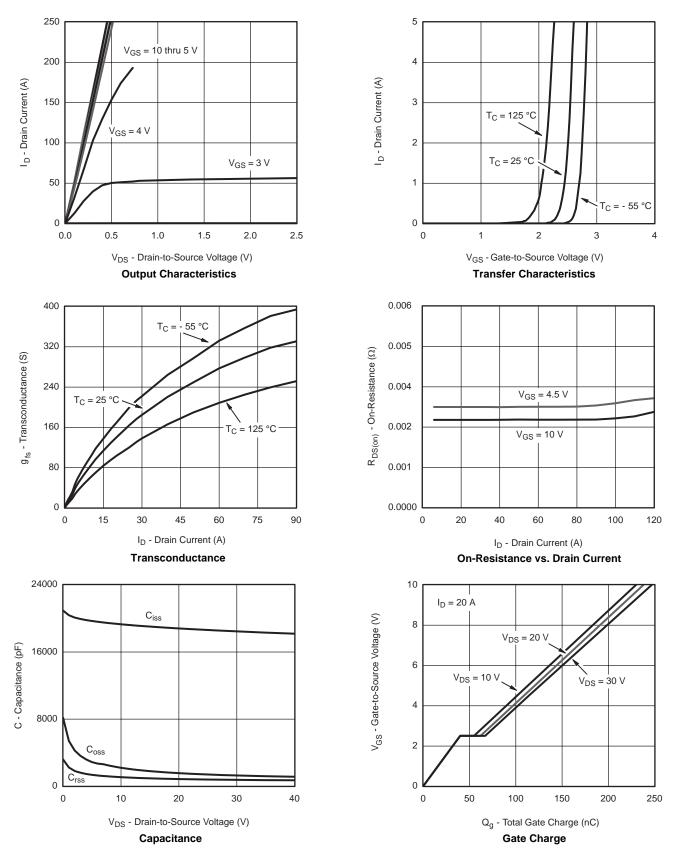
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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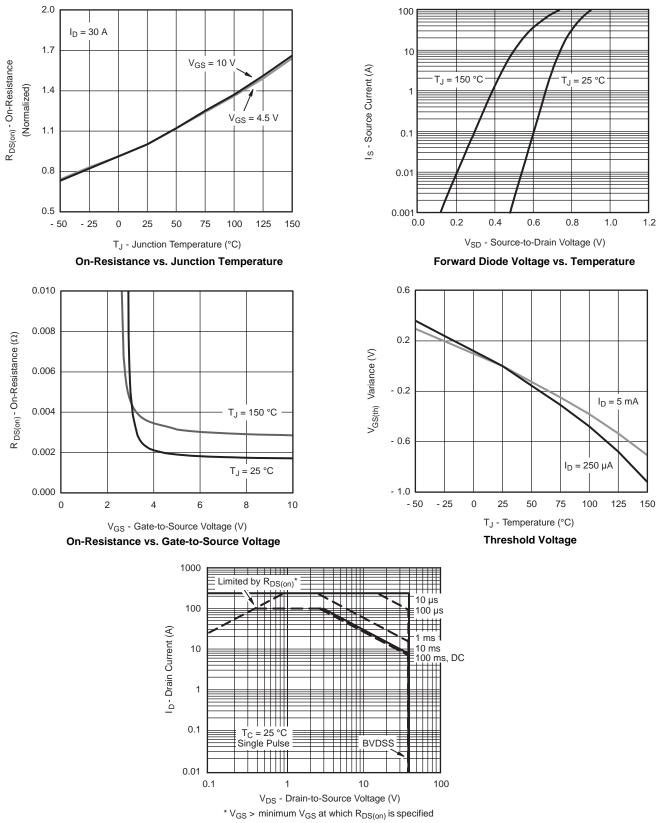
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



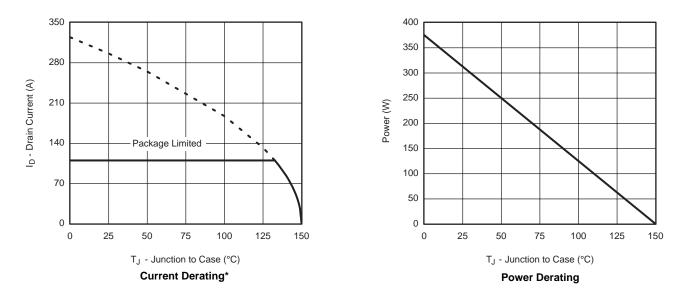
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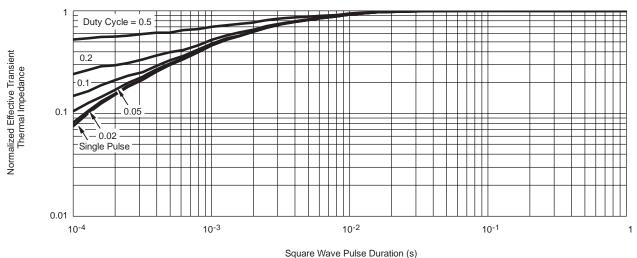






TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

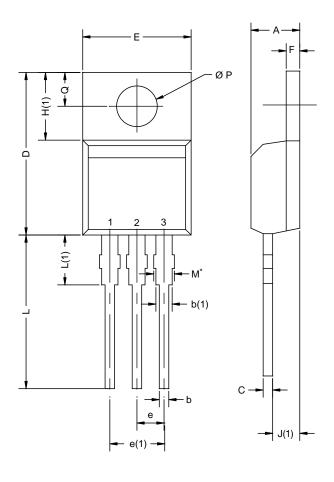
* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220AB



DIM.	MILLIM	IETERS	INCHES		
	MIN.	MAX.	MIN.	MAX	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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