

KIA740H-VB Datasheet

N-Channel 500V (D-S)Super Junction Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V) at T _J max.	500
R _{DS(on)} at 25 °C (Ω)	V _{GS} = 10 V 0.380
Q _g max. (nC)	50
Q _{gs} (nC)	6
Q _{gd} (nC)	10
Configuration	Single

FEATURES

- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)

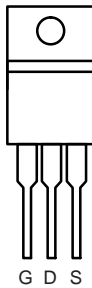
APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics

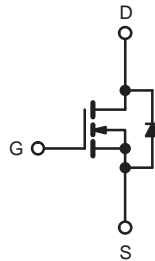


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Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	500	V	
Gate-Source Voltage	V _{GS}	± 30		
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	11	A
		T _C = 100 °C	6.6	
Pulsed Drain Current ^a	I _{DM}	21		
Linear Derating Factor		0.91	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}	103	mJ	
Maximum Power Dissipation	P _D	114	W	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	dV/dt	V _{DS} = 0 V to 80 % V _{DS}	70	V/ns
Reverse Diode dV/dt ^d		27		
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 2.7 A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.1	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.60	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 6 A	-	0.380	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 6 A		-	3.1	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	886	-	pF
Output Capacitance	C _{oss}			-	52	-	
Reverse Transfer Capacitance	C _{rss}			-	6	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}			-	45	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	131	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6 A, V _{DS} = 400 V	-	25	50	nC
Gate-Source Charge	Q _{gs}			-	6	-	
Gate-Drain Charge	Q _{gd}			-	10	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	13	26	ns
Rise Time	t _r			-	16	32	
Turn-Off Delay Time	t _{d(off)}			-	29	58	
Fall Time	t _f			-	12	24	
Gate Input Resistance	R _g			f = 1 MHz, open drain		-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	11	A
Pulsed Diode Forward Current	I _{SM}			-	-	21	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 6 A, dI/dt = 100 A/μs, V _R = 25 V		-	244	-	ns
Reverse Recovery Charge	Q _{rr}			-	2.5	-	μC
Reverse Recovery Current	I _{RRM}			-	19	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

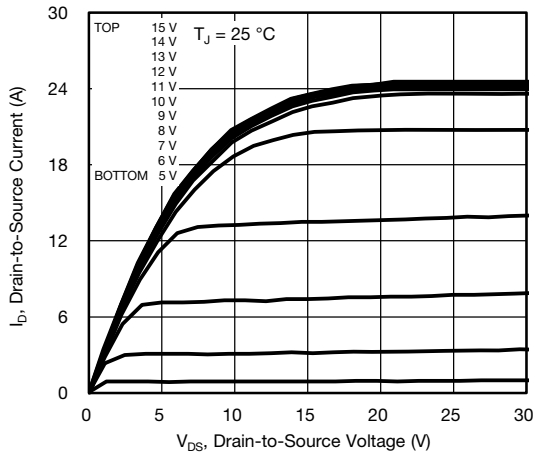


Fig. 1 - Typical Output Characteristics

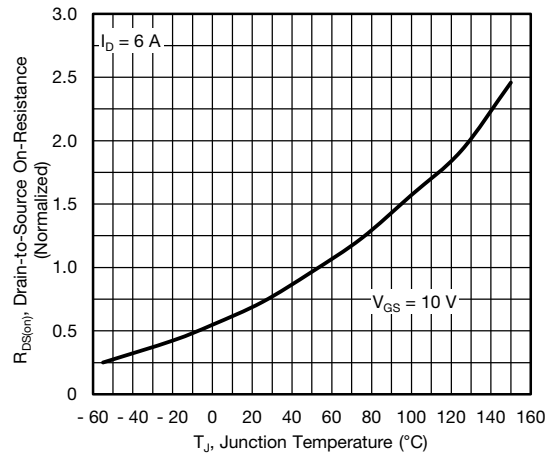


Fig. 4 - Normalized On-Resistance vs. Temperature

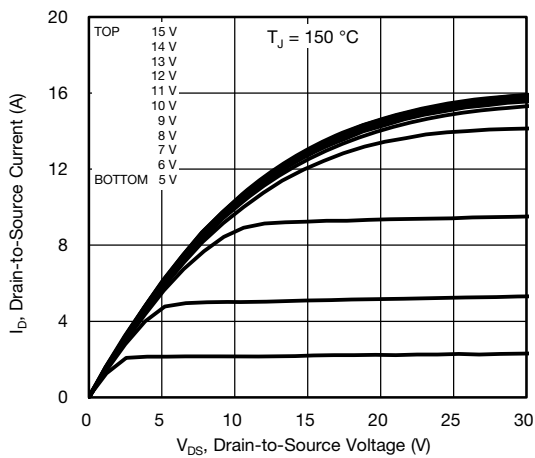


Fig. 2 - Typical Output Characteristics

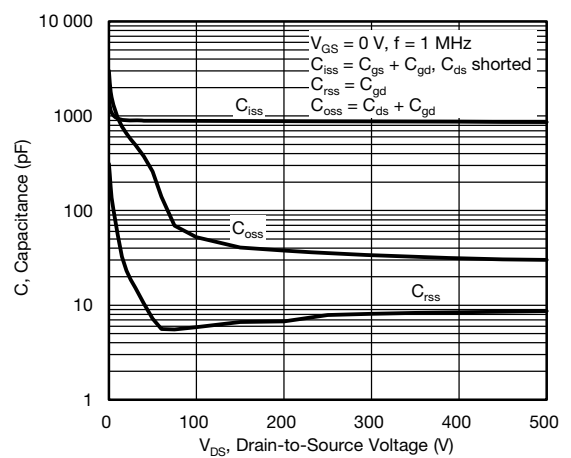


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

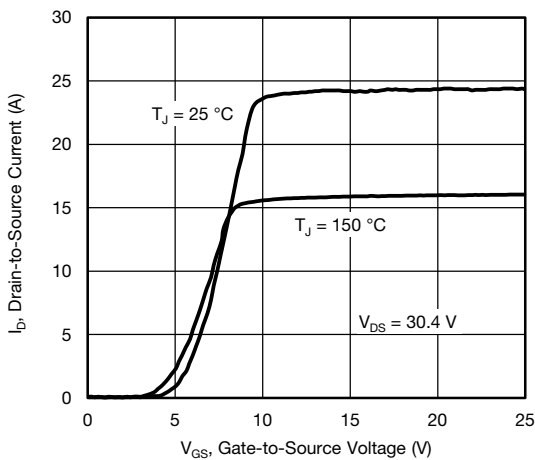


Fig. 3 - Typical Transfer Characteristics

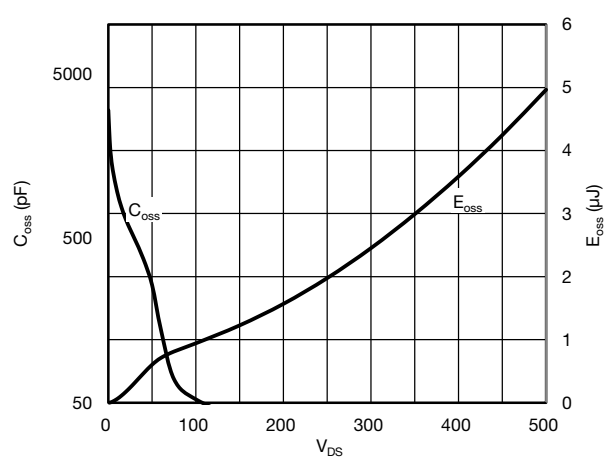


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

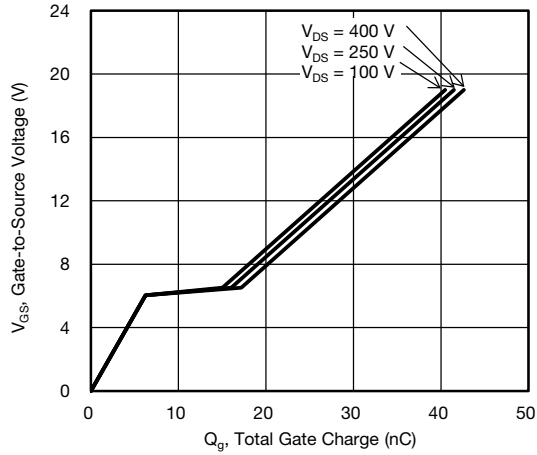


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

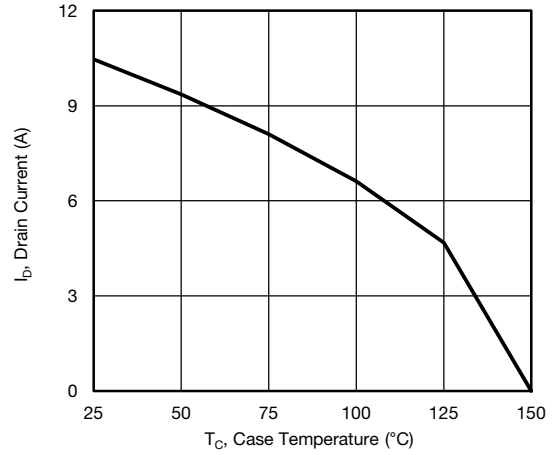


Fig. 10 - Maximum Drain Current vs. Case Temperature

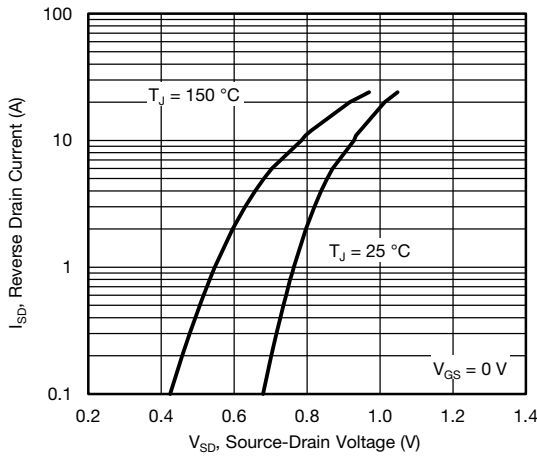


Fig. 8 - Typical Source-Drain Diode Forward Voltage

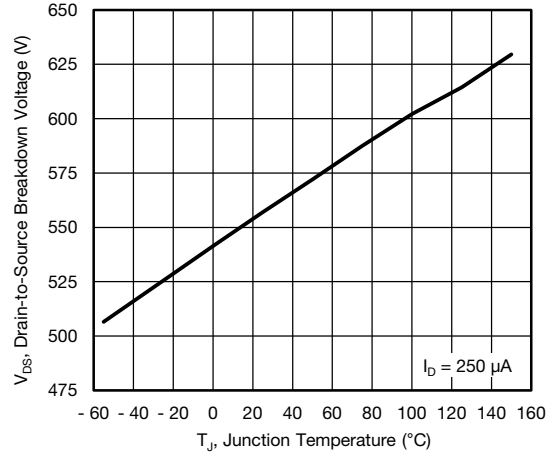


Fig. 11 - Temperature vs. Drain-to-Source Voltage

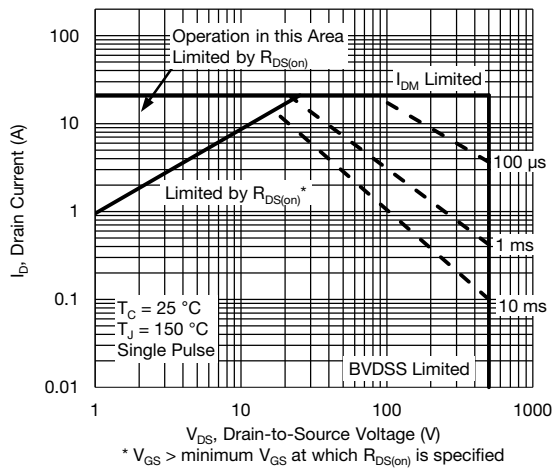


Fig. 9 - Maximum Safe Operating Area

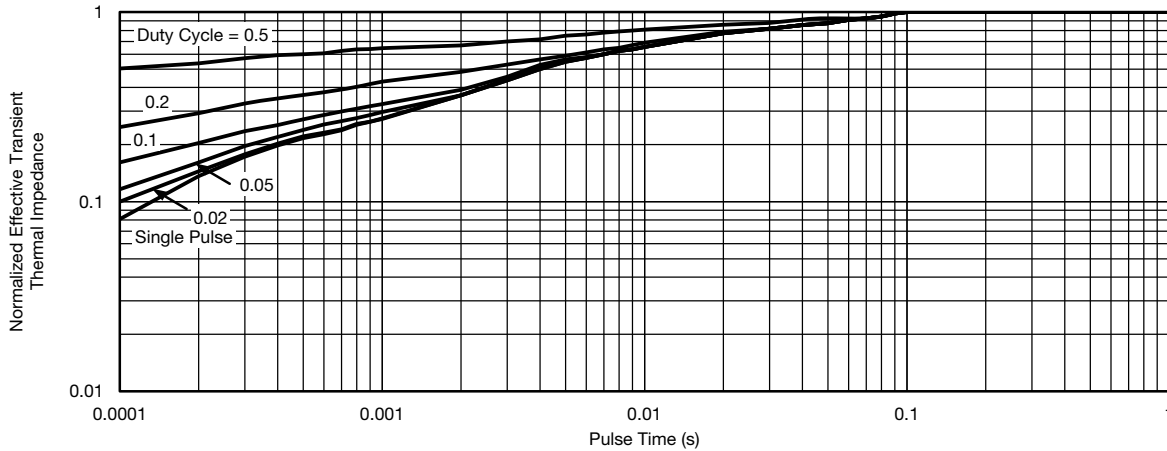


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

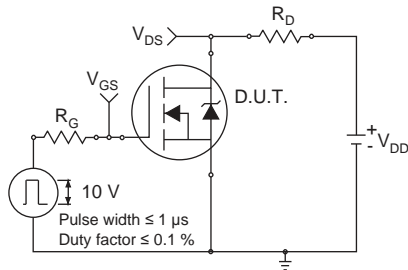


Fig. 13 - Switching Time Test Circuit

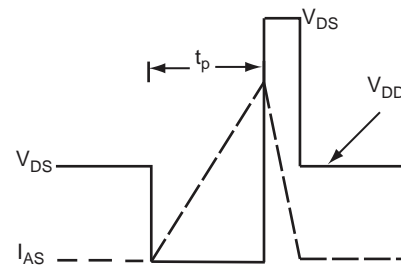


Fig. 16 - Unclamped Inductive Waveforms

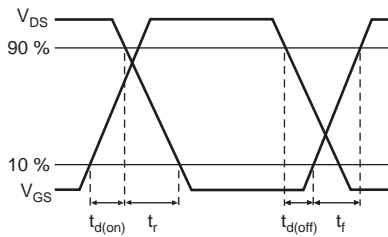


Fig. 14 - Switching Time Waveforms

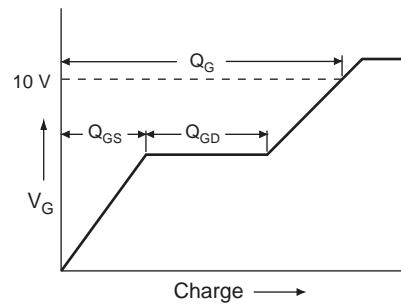


Fig. 17 - Basic Gate Charge Waveform

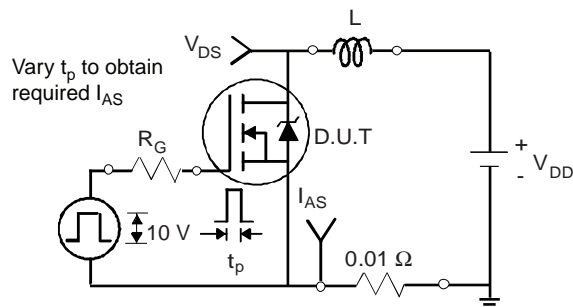


Fig. 15 - Unclamped Inductive Test Circuit

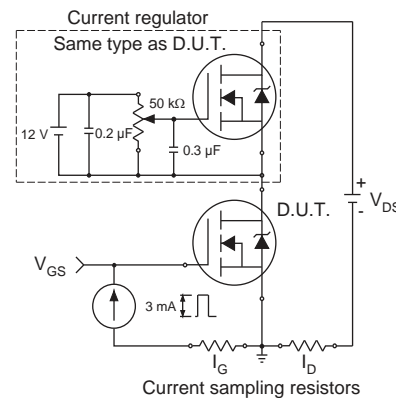
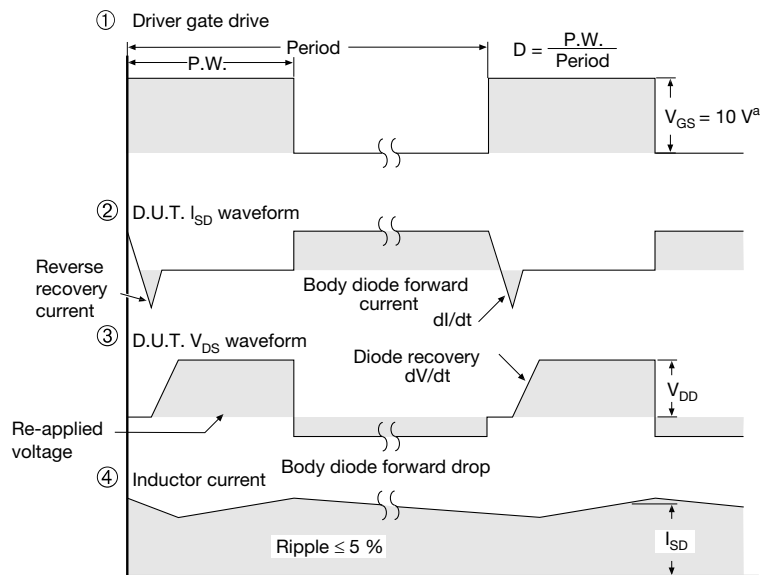
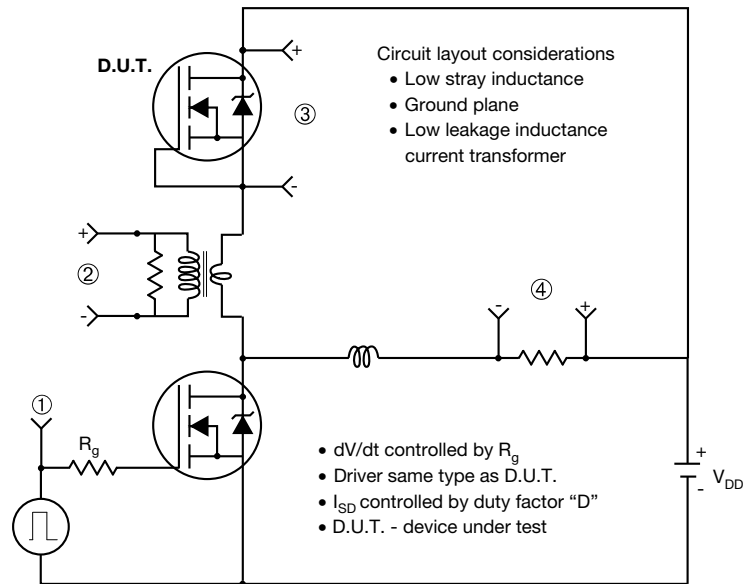


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

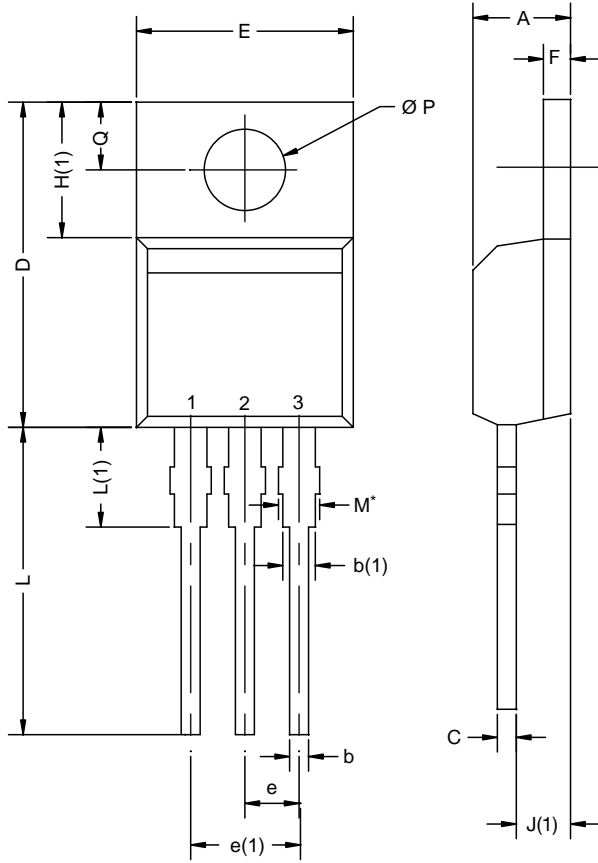


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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