

### **IRFBF30-VB Datasheet**

## N-Channel 900V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	900			
$R_{DS(on)}(\Omega)$	V <sub>GS</sub> = 10 V	1.3		
Q <sub>g</sub> (Max.) (nC)	200			
Q <sub>gs</sub> (nC)	24			
Q <sub>gd</sub> (nC)	110			
Configuration	Single			

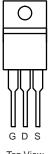
#### **FEATURES**

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- · Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

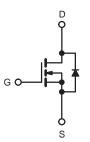




#### TO-220AB



Top View



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			$V_{DS}$	900	V	
Gate-Source Voltage			$V_{GS}$	± 20	7 v	
Continuous Drain Current	$V_{GS}$ at 10 V $T_C = 25 ^{\circ}\text{C}$	L-	5			
	VGS at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	3.9	Α	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	21		
Linear Derating Factor				1.5	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	770	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	7.8	А	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	19	mJ	
Maximum Power Dissipation $T_C = 25  ^{\circ}C$			$P_{D}$	190	W	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	2.0	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	7	
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
				1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD}=50~V$ , starting  $T_J=25~^{\circ}C$ , L=23~mH,  $R_g=25~\Omega$ ,  $I_{AS}=7.8~A$  (see fig. 12). c.  $I_{SD}\leq 7.8~A$ ,  $dI/dt\leq 140~A/\mu s$ ,  $V_{DD}\leq 600~V$ ,  $T_J\leq 150~^{\circ}C$ . d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	40			
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.24	-	°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	0.65			

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						,	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		900	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I <sub>D</sub> = 1 mA	-	0.98	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> :	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zoro Cata Voltago Prain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V		-	-	100	μΑ
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 640 \	V <sub>DS</sub> = 640 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	$I_D = 3.7 \text{ A}^b$	-	1.3	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =	: 100 V, I <sub>D</sub> = 3.7 A <sup>b</sup>	5.6	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 V,		3100	-	
Output Capacitance	C <sub>oss</sub>	1	$V_{DS} = 25 \text{ V},$	-	800	-	рF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1	f = 1.0 MHz, see fig. 5		490	-	
Total Gate Charge	$Q_g$			-	-	200	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{GS} = 10 \text{ V}$	$V_{GS} = 10 \text{ V}$ $I_D = 3.8 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 <sup>b</sup>		-	24	
Gate-Drain Charge	$Q_{gd}$				-	110	
Turn-On Delay Time	t <sub>d(on)</sub>				19	-	- - ns
Rise Time	t <sub>r</sub>	$V_{DD} = 400 \text{ V, } I_{D} = 3.8 \text{ A,}$ $R_{g} = 6.2 \Omega, R_{D} = 52 \Omega$ see fig. $10^{b}$		-	38	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	120	-	
Fall Time	t <sub>f</sub>			-	39	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	mll
Internal Source Inductance	L <sub>S</sub>			-	13	-	- nH
Drain-Source Body Diode Characteristic	s					•	
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.0	
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	21	A
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C	$I_{S} = 3.8 \text{ A}, V_{GS} = 0 \text{ V}^{b}$	-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.8 A, dl/dt = 100 A/μs <sup>b</sup>		-	650	980	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	3.8	5.7	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by $L_{\rm S}$ and $L_{\rm C}$				L <sub>D</sub> )	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %.



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

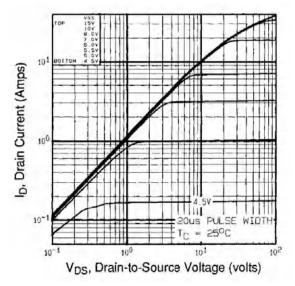


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

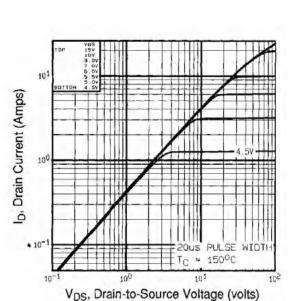


Fig. 2 - Typical Output Characteristics,  $T_C$  = 150 °C

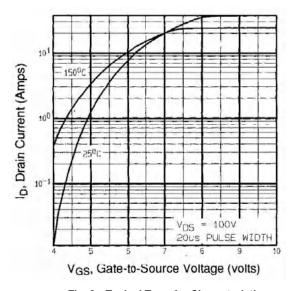


Fig. 3 - Typical Transfer Characteristics

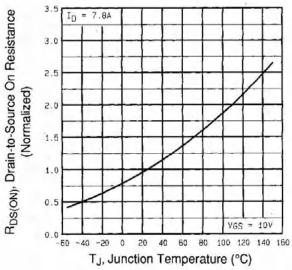


Fig. 4 - Normalized On-Resistance vs. Temperature



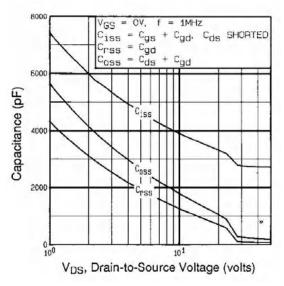


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

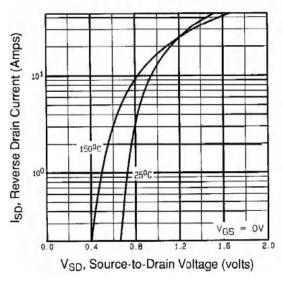


Fig. 7 - Typical Source-Drain Diode Forward Voltage

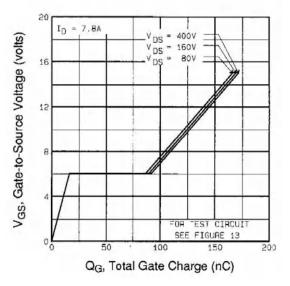


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

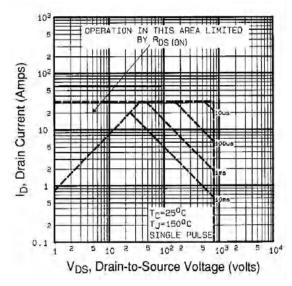


Fig. 8 - Maximum Safe Operating Area



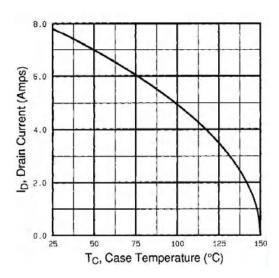


Fig. 9 - Maximum Drain Current vs. Case Temperature

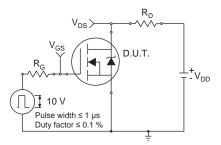


Fig. 10a - Switching Time Test Circuit

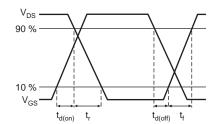


Fig. 10b - Switching Time Waveforms

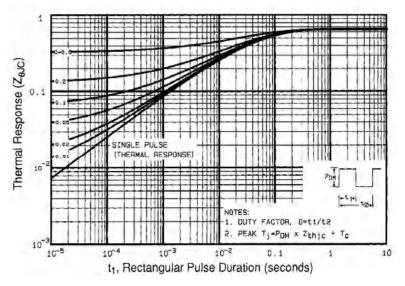


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



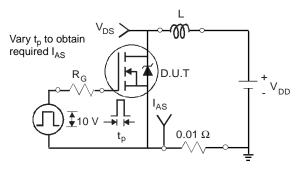


Fig. 12a - Unclamped Inductive Test Circuit

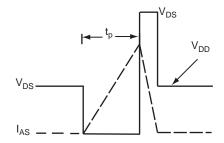


Fig. 12b - Unclamped Inductive Waveforms

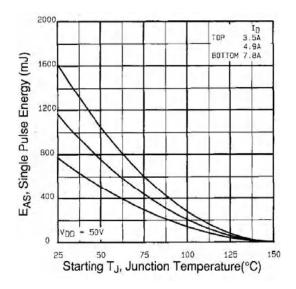


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

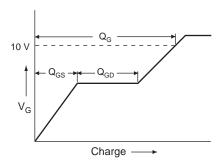


Fig. 13a - Basic Gate Charge Waveform

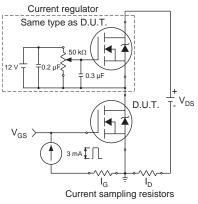
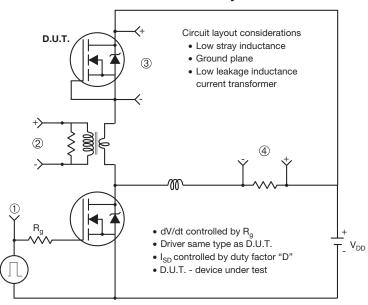


Fig. 13b - Gate Charge Test Circuit



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#### Peak Diode Recovery dV/dt Test Circuit



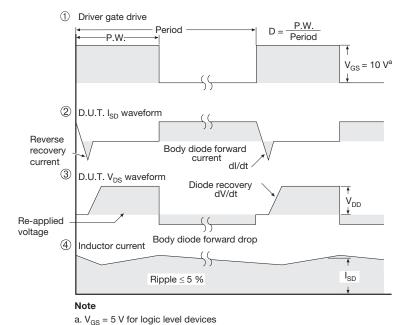
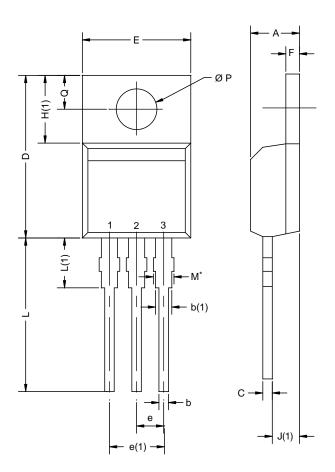


Fig. 14 - For N-Channel



### **TO-220AB**



	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471					

#### Notes

 $<sup>^{\</sup>star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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