

HM740-VB Datasheet

N-Channel 650V (D-S) Super Junction Power MOSFET

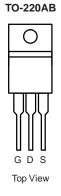
PRODUCT SUMMARY				
V_{DS} (V) at T_J max.	700			
R _{DS(on)} at 25 °C (Ω)	V _{GS} = 10 V 0.5			
Q _g max. (nC)	25			
Q _{gs} (nC)	2.0			
Q _{gd} (nC)	2.7			
Configuration	Single			

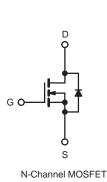
FEATURES

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Qg)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial





PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	
Gate-Source Voltage			V _{GS}	± 30	- V
Continuous Durin Current (T. 150 °C)		T _C = 25 °C		9	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	$V_{GS} \text{ at } 10 \text{ V} \qquad \frac{T_{C} = 25 \text{ °C}}{T_{C} = 100 \text{ °C}}$	ID	6	А
Pulsed Drain Current ^a			I _{DM}	21	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	186	mJ
Maximum Power Dissipation			PD	123	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope $T_J = 125 \text{ °C}$		dV/dt	50	V/ns	
Reverse Diode dV/dt ^d			uv/di	4.5	v/ns
Soldering Recommendations (Peak Temperature) c for 10 s			300	°C	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature. b. $V_{DD} = 50 \text{ V}$, starting $T_J = 25 \text{ °C}$, L = 28.2 mH, $R_g = 25 \Omega$, $I_{AS} = 3.5 \text{ A}$. c. 1.6 mm from case. d. $I_{SD} \le I_D$, dI/dt = 100 A/µs, starting $T_J = 25 \text{ °C}$.



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	63	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.6	0/11	

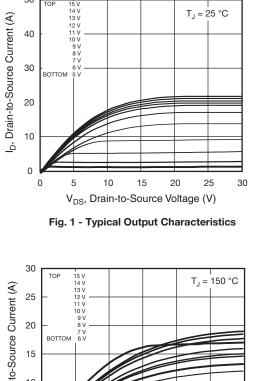
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 250 μA	650	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.65	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μΑ	2	-	4	V
	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Gate-Source Leakage		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
			$V_{DS} = 600 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$		-	1	+ -
Zero Gate Voltage Drain Current	I _{DSS}		∕, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 4 A$	-	0.50	-	Ω
Forward Transconductance	g _{fs}	V _{DS}	= 30 V, I _D = 4 A	-	16	-	S
Dynamic		•					1
Input Capacitance	C _{iss}		V _{GS} = 0 V,	-	360	-	
Output Capacitance	C _{oss}	-	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$ f = 1 MHz		25	-	pF
Reverse Transfer Capacitance	C _{rss}	-			12	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	$V_{DS} = 0$ V to 520 V, $V_{GS} = 0$ V		-	45	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	62	-	
Total Gate Charge	Qg				25		nC
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V I _D = 4 A, V _{DS} = 520 V		-	2.0	-	
Gate-Drain Charge	Q _{gd}			-	2.7	-	1
Turn-On Delay Time	t _{d(on)}	V_{DD} = 520 V, I _D = 4 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	25	-	ns
Rise Time	t _r			-	55	-	
Turn-Off Delay Time	t _{d(off)}			-	70	-	
Fall Time	t _f				40	-	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	3.5	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	7	
Pulsed Diode Forward Current	I _{SM}			-	-	18	A
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 4 A, V _{GS} = 0 V		-	-	1.5	V
Reverse Recovery Time	t _{rr}	$T_{J} = 25 \text{ °C}, I_{F} = I_{S} = 4 \text{ A}, \\ dI/dt = 100 \text{ A/}\mu\text{s}, V_{R} = 400 \text{ V}$		-	190	-	ns
Reverse Recovery Charge	Q _{rr}			-	2.3	-	μC
Reverse Recovery Current	I _{BRM}				10		A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

50





TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

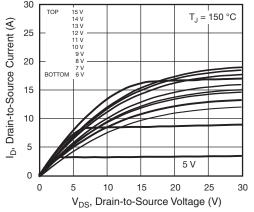


Fig. 2 - Typical Output Characteristics

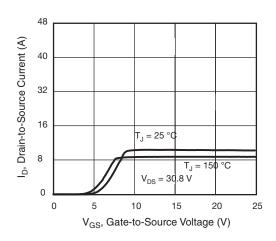


Fig. 3 - Typical Transfer Characteristics

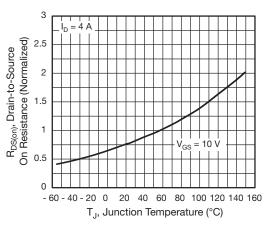


Fig. 4 - Normalized On-Resistance vs. Temperature

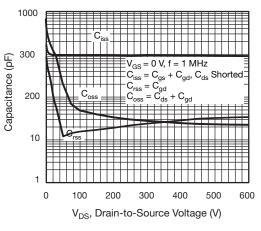


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

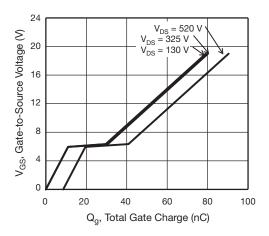


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

HM740-VB



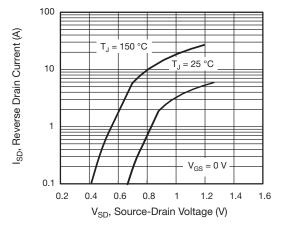


Fig. 7 - Typical Source-Drain Diode Forward Voltage

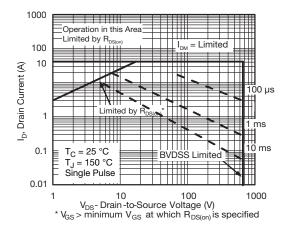


Fig. 8 - Maximum Safe Operating Area

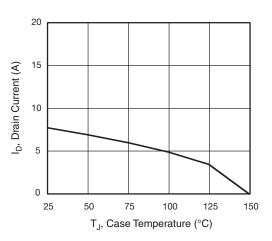


Fig. 9 - Maximum Drain Current vs. Case Temperature

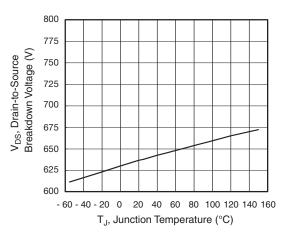


Fig. 10 - Temperature vs. Drain-to-Source Voltage

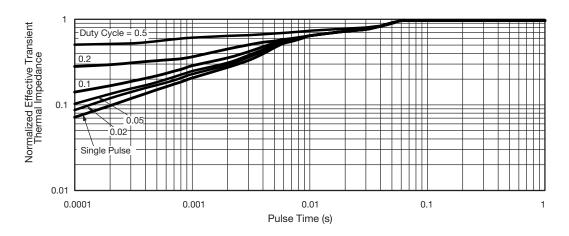


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



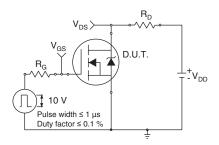


Fig. 12 - Switching Time Test Circuit

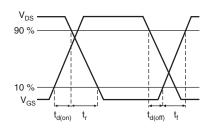


Fig. 13 - Switching Time Waveforms

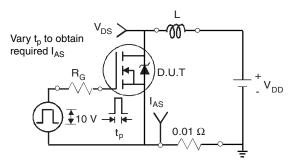


Fig. 14 - Unclamped Inductive Test Circuit

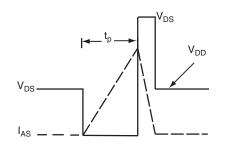


Fig. 15 - Unclamped Inductive Waveforms

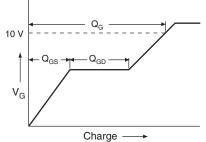


Fig. 16 - Basic Gate Charge Waveform

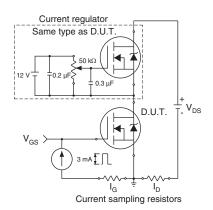
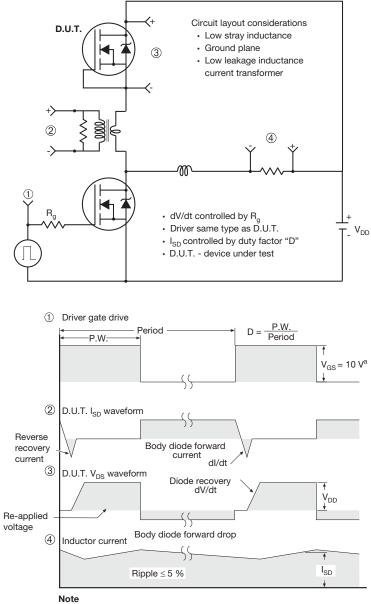


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit

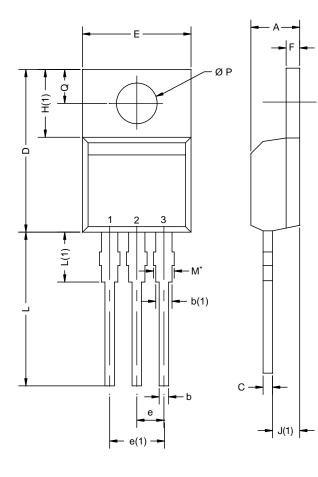


a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel



TO-220AB



	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12-0 DWG: 5471	0208-Rev. N, I	08-Oct-12			

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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