

# FB5615-VB Datasheet N-Channel 150-V (D-S) 175 °C MOSFET

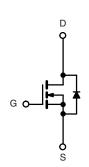
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A)		
150	0.030 at V <sub>GS</sub> = 10 V	50		
150	0.033 at V <sub>GS</sub> = 6 V	45		

#### FEATURES

- TrenchFET<sup>®</sup> Power MOSFETs
- 175 °C Junction Temperature
- New Low Thermal Resistance Package
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

• Primary Side Switch



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_{C}$ = 25 °C, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	150	v	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current ( $T_1 = 175 \ ^{\circ}C$ )	T <sub>C</sub> = 25 °C	1-	50		
Continuous Drain Current $(1) = 175^{\circ} C$	T <sub>C</sub> = 125 °C	I <sub>D</sub>	35	A	
Pulsed Drain Current	I <sub>DM</sub>	150	A		
Avalanche Current		I <sub>AR</sub>	50		
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	80	mJ	
	T <sub>C</sub> = 25 °C	Р	166 <sup>b</sup>	14/	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C <sup>c</sup>	– P <sub>D</sub> –	3.75	- W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

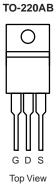
THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient <sup>c</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.9	0/10		

Notes:

a. Duty cycle  $\leq$  1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).







Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{DS} = 0 V, I_{D} = 250 \mu A$	150			V	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2		4	v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 120 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V		1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 120 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$			50 μΑ		
		$V_{DS}$ = 120 V, $V_{GS}$ = 0 V, $T_{J}$ = 175 °C			250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	80			Α	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.030			
	P	$V_{GS} = 6 V, I_{D} = 10 A$		0.033		0	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS}$ = 10 V, $I_{D}$ = 15 A, $T_{J}$ = 125 °C		0.076		Ω	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C		0.100			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	10			S	
Dynamic <sup>b</sup>	+			+			
Input Capacitance	C <sub>iss</sub>			2500		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz		290			
Reverse Transfer Capacitance	C <sub>rss</sub>			190			
Gate Resistance	Rg			2		Ω	
Total Gate Charge <sup>c</sup>	Qg			38	60	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$		13			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			13			
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 75 V, R <sub>L</sub> = 1.80 Ω		130	200		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 40 A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 2.5 $\Omega$		30	45	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>			90	140	1	
Source-Drain Diode Ratings and Cha	racteristics 7	Γ <sub>C</sub> = 25 °C <sup>b</sup>					
Continuous Current	۱ <sub>S</sub>				40		
Pulsed Current	I <sub>SM</sub>			1	80	A	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{F} = 40 \text{ A}, V_{GS} = 0 \text{ V}$		1.0	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>			100	150	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 40 A, dl/dt = 100 A/μs		5	8	Α	
Reverse Recovery Charge	Q <sub>rr</sub>			0.25	0.6	μC	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 % b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

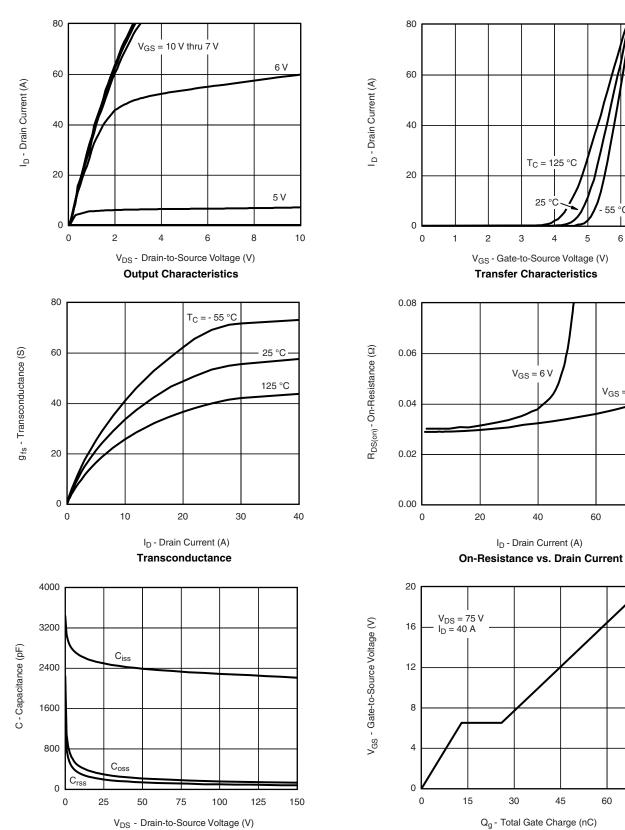
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



55 °C

 $V_{GS} = 10 V$ 

Gate Charge



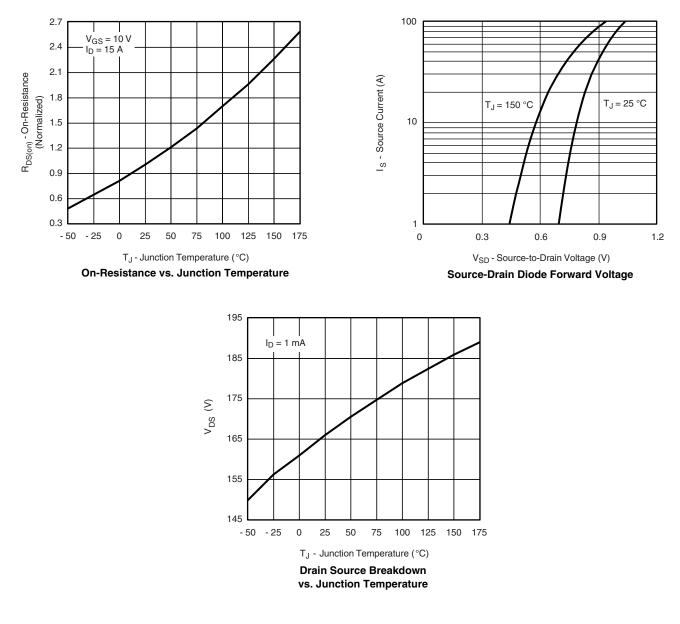
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

服务热线:400-655-8788

Capacitance

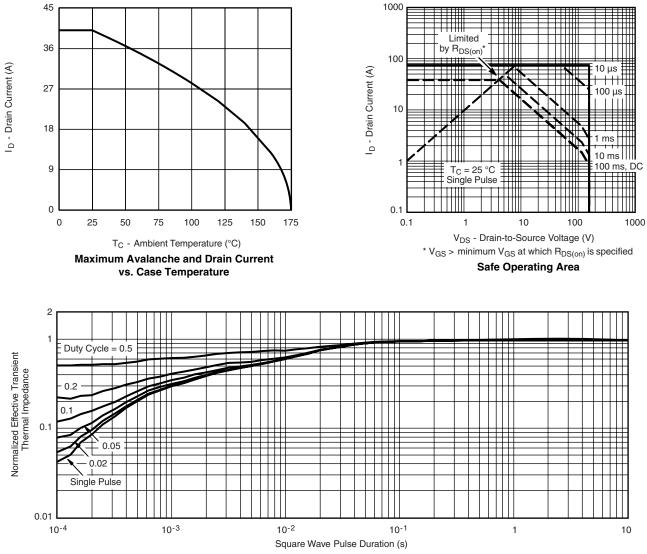


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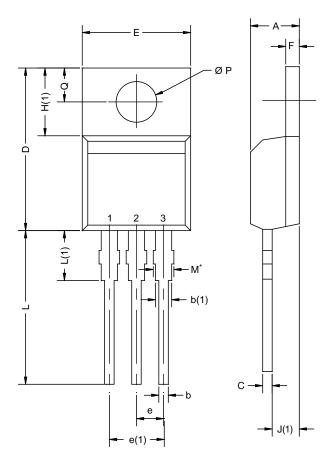
#### THERMAL RATINGS



Normalized Thermal Transient Impedance, Junction-to-Case



### **TO-220AB**



	MILLIN	IETERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
с	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØР	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: X12- DWG: 547	0208-Rev. N, 1	08-Oct-12			

#### Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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