

### F650A-VB Datasheet

# N-Channel 200 V (D-S) MOSFET

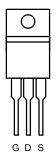
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)		
200	0.058at V <sub>GS</sub> = 10 V	35		

#### **FEATURES**

- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- New Low Thermal Resistance Package
- · Compliant to RoHS Directive 2002/95/EC

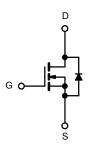


#### TO-220AB



#### **APPLICATIONS**

Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	<b>S</b> ( $T_C = 25  ^{\circ}C$ , unless oth	nerwise noted)		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	200	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T, = 175 °C)	T <sub>C</sub> = 25 °C	1-	35	
Continuous Diain Current (1) = 173 C)	T <sub>C</sub> = 125 °C	I <sub>D</sub>	23	
Pulsed Drain Current	I <sub>DM</sub>	70	Α Α	
Avalanche Current		I <sub>AR</sub>	35	
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	61	mJ
Manipular Danier Disable Africa	T <sub>C</sub> = 25 °C	В	300 <sup>b</sup>	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C <sup>c</sup>	$ P_D$ $-$	3.75	vv
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.5	C/VV	

#### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).



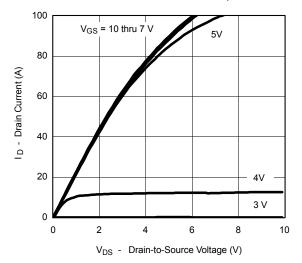
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Parameter	Symbol	Test Conditions	Min .	Тур.	Max.	Unit	
Static Project		V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	000				
Drain-Source Breakdown Voltage	V <sub>DS</sub>	50 5 1	200			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4		
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 30 V			± 250	nA	
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V				1 50 μΑ	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$					
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α	
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.058			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DQ</sub> ,	$V_{GS}$ = 10 V, $I_{D}$ = 20 A, $T_{J}$ = 125 °C		0.130		Ω	
Dialii-Source Oil-State Resistance	R <sub>DS(on)</sub>	$V_{GS}$ = 10 V, $I_{D}$ = 20 A, $T_{J}$ = 175 °C		0.170			
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 15 A		0.070			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		70		S	
Dynamic <sup>b</sup>	•			•			
Input Capacitance	C <sub>iss</sub>			2690		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		200			
Reverse Transfer Capacitance	C <sub>rss</sub>			110			
Total Gate Charge <sup>c</sup>	$Q_g$			95	140		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 45 A		28		nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			34			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.6		Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			22	35		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 100 \text{ V}, R_1 = 2.78 \Omega$		220	330		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 45 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		40	60	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>			145	220		
Source-Drain Diode Ratings and Cha	aracteristics (	T <sub>C</sub> = 25 °C) <sup>b</sup>					
Continuous Current	I <sub>S</sub>				45		
Pulsed Current	I <sub>SM</sub>		70		70	_ A	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 V		1	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>	. 55		150	225	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 45 A, di/dt = 100 A/μs		12	18	Α	
Reverse Recovery Charge	Q <sub>rr</sub>			0.9	2	uС	

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

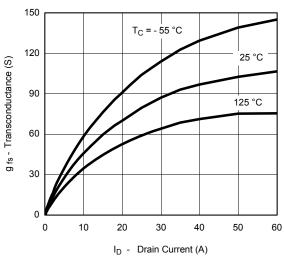
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



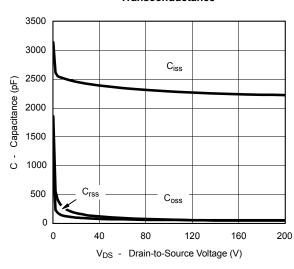
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



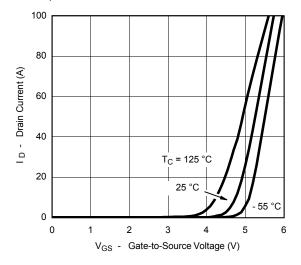
#### **Output Characteristics**



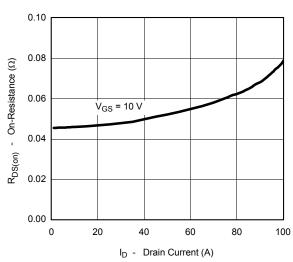
#### Transconductance



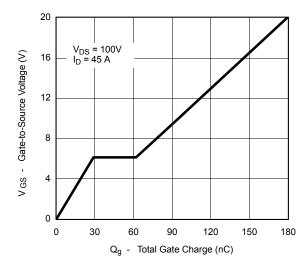
#### Capacitance



#### **Transfer Characteristics**



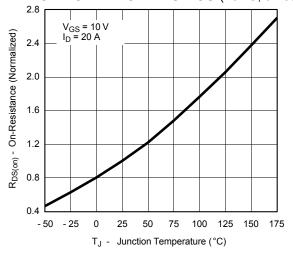
#### On-Resistance vs. Drain Current



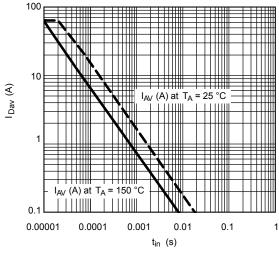
**Gate Charge** 



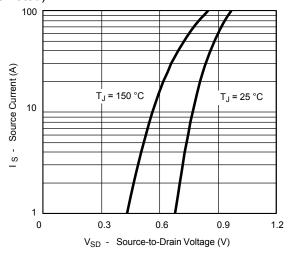
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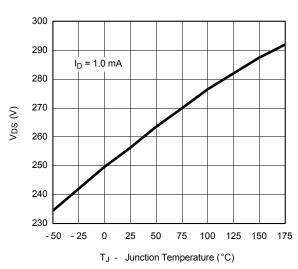
#### On-Resistance vs. Junction Temperature



**Avalanche Current vs. Time** 



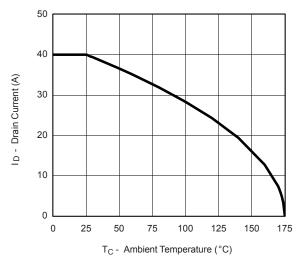
Source-Drain Diode Forward Voltage

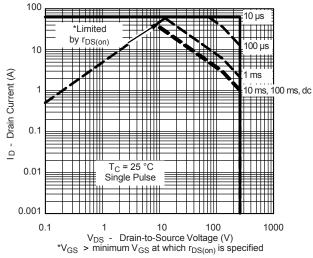


Drain Source Breakdown vs. Junction Temperature



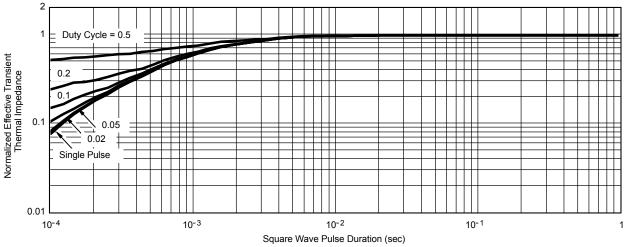
#### THERMAL RATINGS





Maximum Avalanche and Drain Current vs. Case Temperature

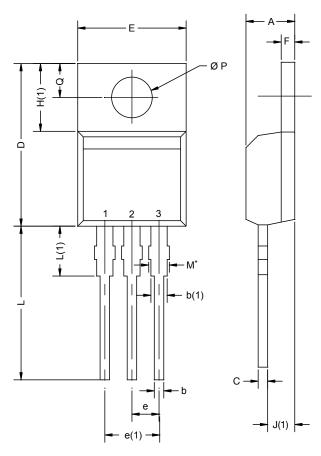
Safe Operating Area, Case Temperature



Normalized Thermal Transient Impedance, Junction-to-Case



# **TO-220AB**



	D2

	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	4.25	4.65	0.167	0.183	
b	0.69	1.01	0.027	0.040	
b(1)	1.20	1.73	0.047	0.068	
С	0.36	0.61	0.014	0.024	
D	14.85	15.49	0.585	0.610	
D2	12.19	12.70	0.480	0.500	
Е	10.04	10.51	0.395	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.09	6.48	0.240	0.255	
J(1)	2.41	2.92	0.095	0.115	
L	13.35	14.02	0.526	0.552	
L(1)	3.32	3.82	0.131	0.150	
ØΡ	3.54	3.94	0.139	0.155	
Q	2.60	3.00	0.102	0.118	
ECN: T14-0413-Rev. P, 16-Jun-14 DWG: 5471					

#### Note

 $^{\star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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