

DTP14N50SJ-VB Datasheet

N-Channel 500-V (D-S) Super Junction MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	500	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.243
Q_g max. (nC)	66	
Q_{gs} (nC)	8	
Q_{gd} (nC)	14	
Configuration	Single	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)

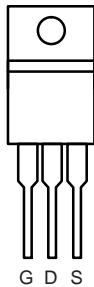


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COMPLIANT
HALOGEN
FREE

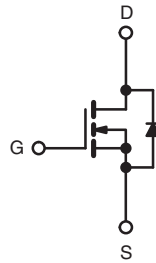
APPLICATIONS

- Computing
- PC silver box / ATX power supplies

TO-220AB



Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	500	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	14.5	A
		$T_C = 100$ °C	9.2	
Pulsed Drain Current ^a	I_{DM}	28		
Linear Derating Factor		1.25	W/°C	
Single Pulse Avalanche Energy ^b	E_{AS}	136	mJ	
Maximum Power Dissipation	P_D	156	W	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	dV/dt	$V_{DS} = 0$ V to 80 % V_{DS}	70	V/ns
Reverse Diode dV/dt ^d		27		
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3.1$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.62	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	10	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	25	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.5 A	-	0.243	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 7.5 A		-	3.9	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	1162	-	pF
Output Capacitance	C _{oss}			-	51	-	
Reverse Transfer Capacitance	C _{rss}			-	7	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}			-	55	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	164	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 7.5 A, V _{DS} = 400 V	-	33	66	nC
Gate-Source Charge	Q _{gs}			-	8	-	
Gate-Drain Charge	Q _{gd}			-	14	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 12 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	15	30	ns
Rise Time	t _r			-	24	48	
Turn-Off Delay Time	t _{d(off)}			-	34	68	
Fall Time	t _f			-	18	36	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.85	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14.5	A
Pulsed Diode Forward Current	I _{SM}			-	-	28	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 7.5 A, di/dt = 100 A/μs, V _R = 25 V		-	265	-	ns
Reverse Recovery Charge	Q _{rr}			-	3.2	-	μC
Reverse Recovery Current	I _{RRM}			-	23	-	A

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

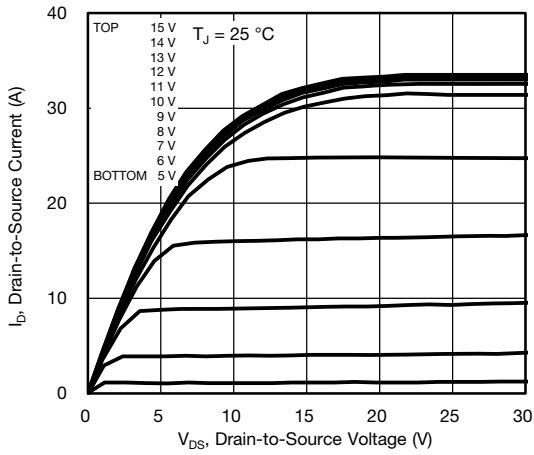


Fig. 1 - Typical Output Characteristics

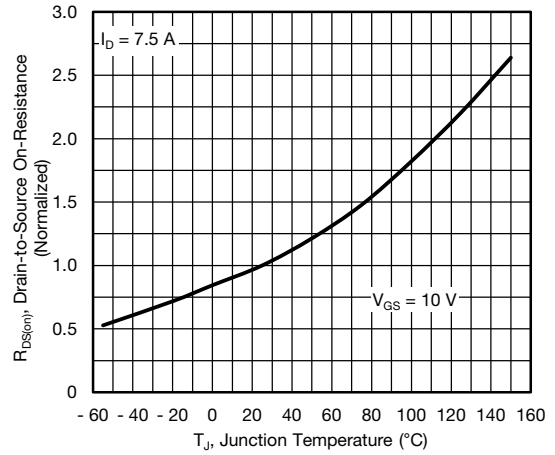


Fig. 4 - Normalized On-Resistance vs. Temperature

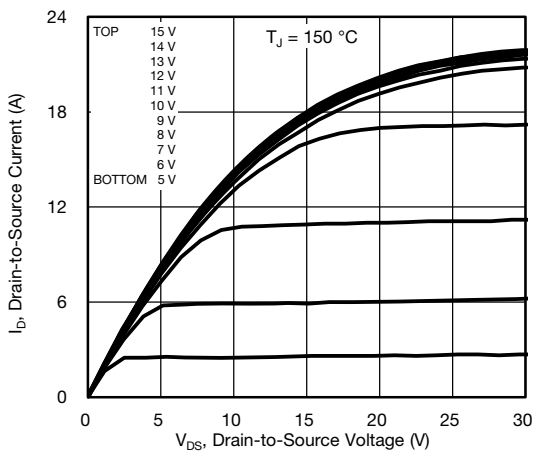


Fig. 2 - Typical Output Characteristics

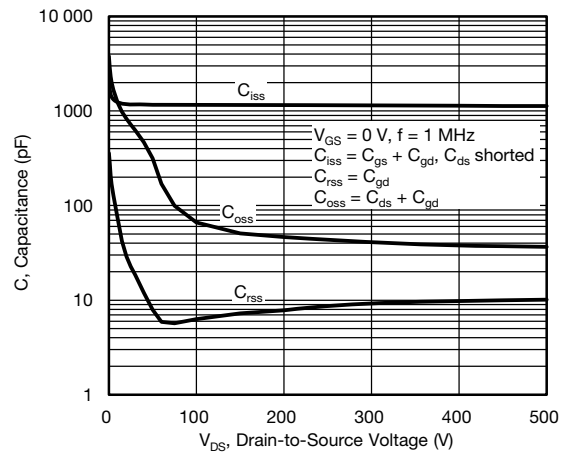


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

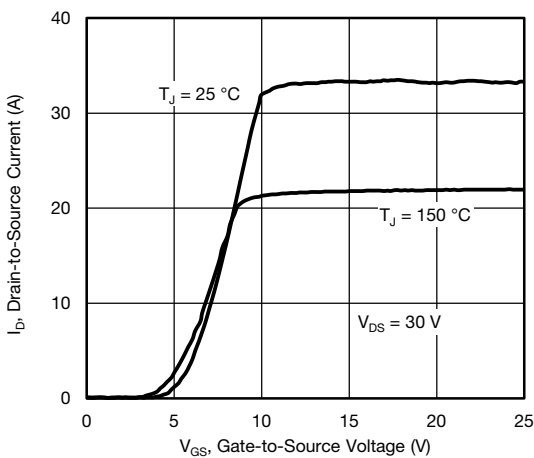


Fig. 3 - Typical Transfer Characteristics

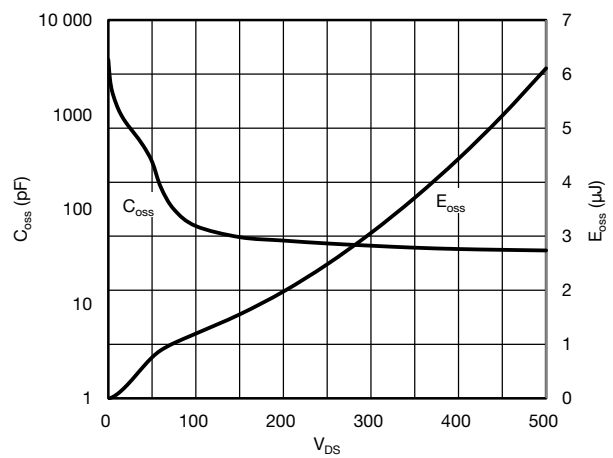


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}

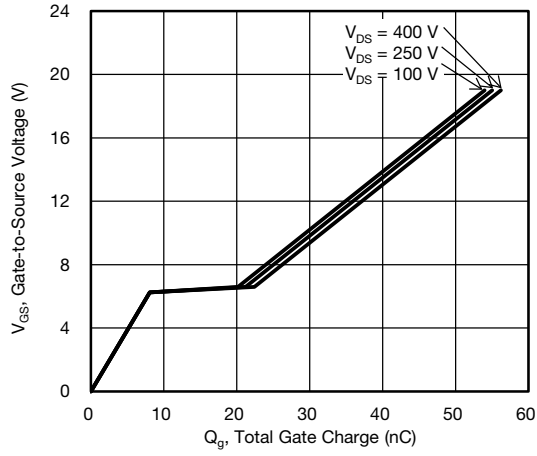


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

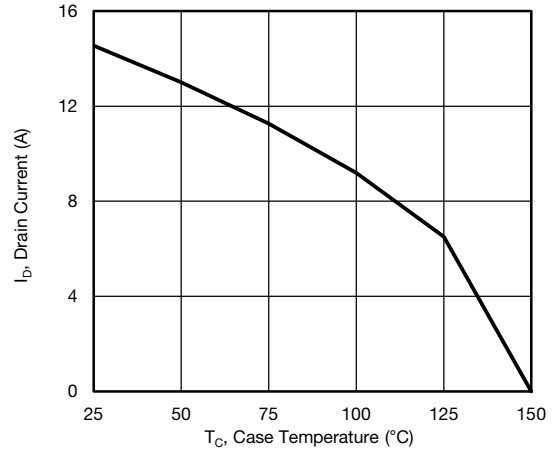


Fig. 10 - Maximum Drain Current vs. Case Temperature

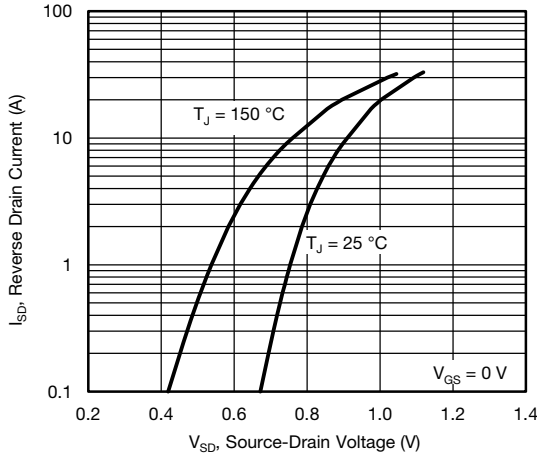


Fig. 8 - Typical Source-Drain Diode Forward Voltage

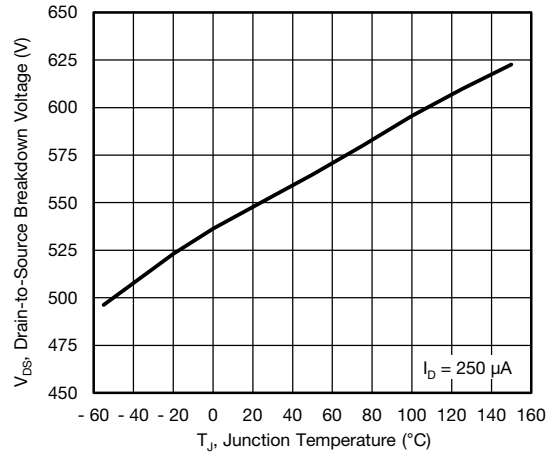


Fig. 11 - Temperature vs. Drain-to-Source Voltage

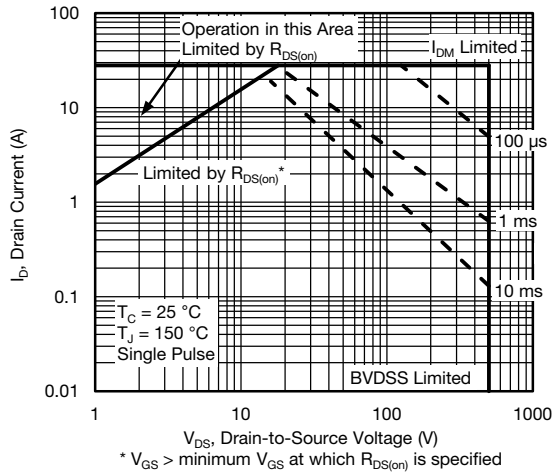


Fig. 9 - Maximum Safe Operating Area

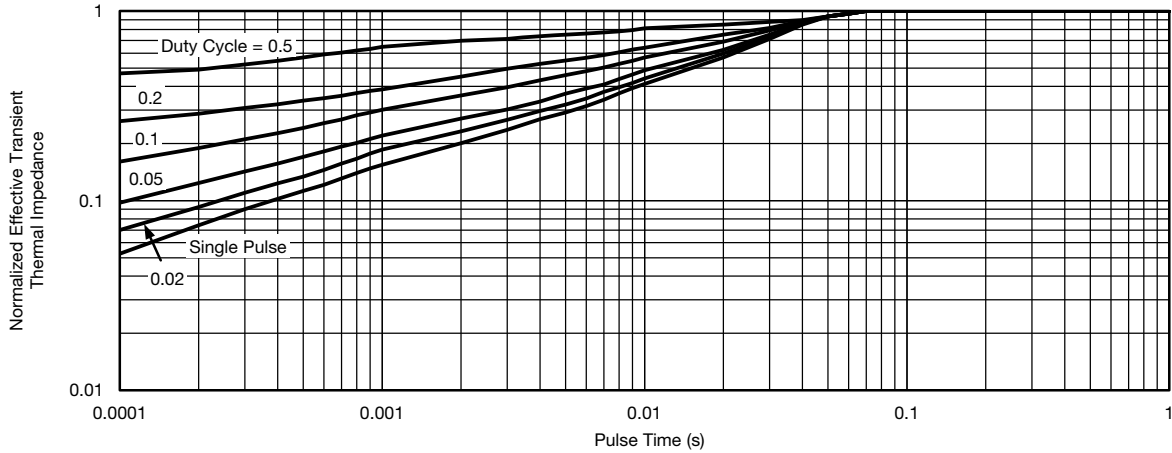


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

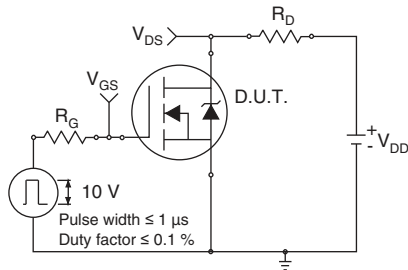


Fig. 13 - Switching Time Test Circuit

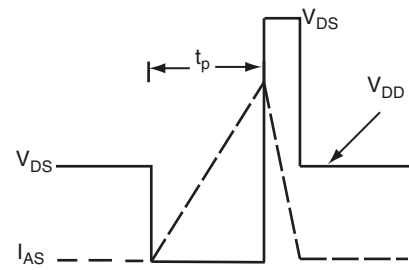


Fig. 16 - Unclamped Inductive Waveforms

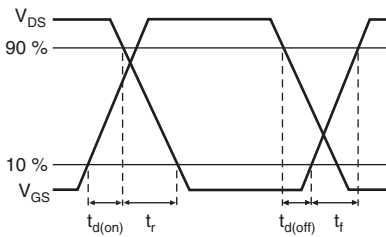


Fig. 14 - Switching Time Waveforms

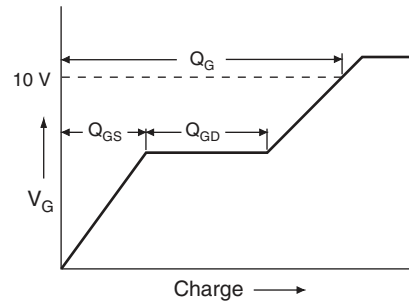


Fig. 17 - Basic Gate Charge Waveform

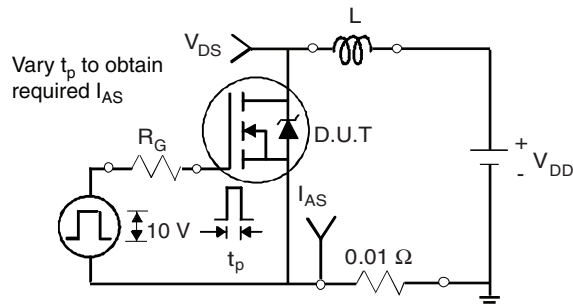


Fig. 15 - Unclamped Inductive Test Circuit

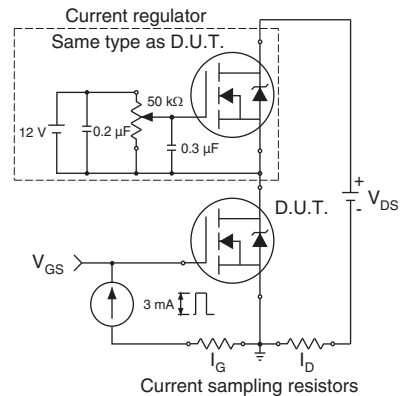
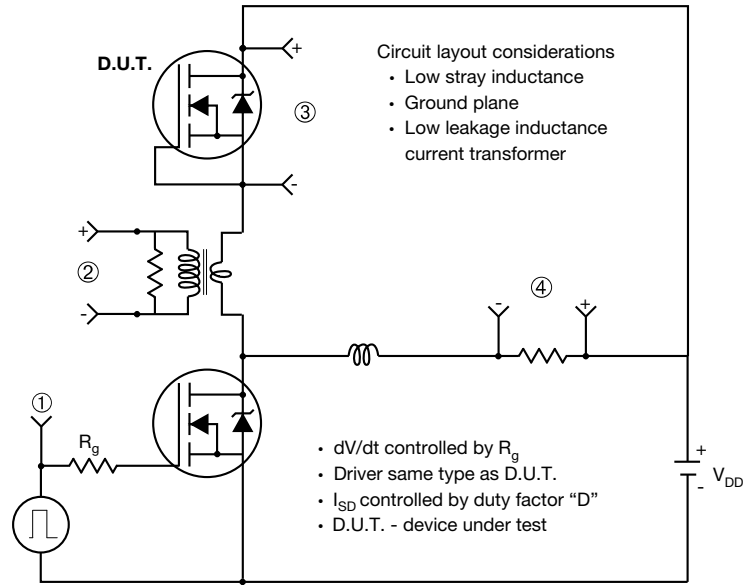


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

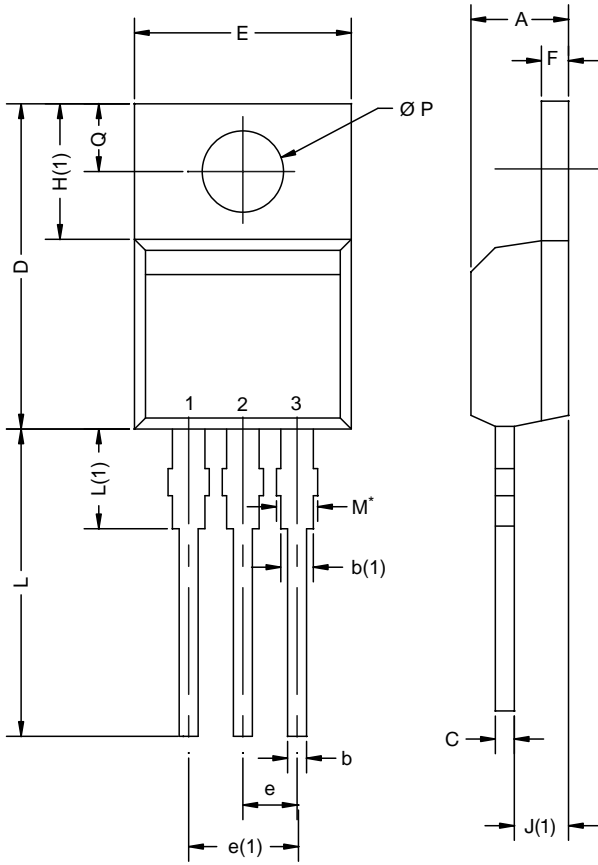


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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