

## SIS412DN-T1-GE3-VB Datasheet N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
30	0.021 at V <sub>GS</sub> = 10 V	18	3.8 nC
	0.025 at V <sub>GS</sub> = 4.5 V	17	

### FEATURES

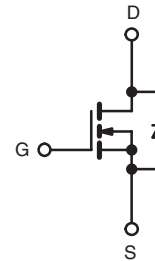
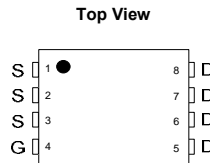
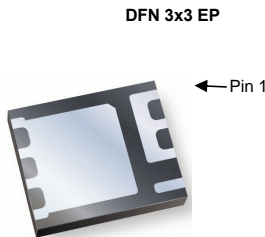
- Halogen-free According to IEC 61249-2-21
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested



**RoHS**  
COMPLIANT

### APPLICATIONS

- Notebook PC
  - System Power
  - Load Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	18 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	11 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	9 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	7 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	35	A	
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	12 <sup>a</sup>	A
		T <sub>A</sub> = 25 °C	2.7 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	5	A	
Single Pulse Avalanche Energy	E <sub>AS</sub>	1.25	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	15.6	W
		T <sub>C</sub> = 70 °C	10	
		T <sub>A</sub> = 25 °C	3.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	32	39	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	6.5	8	°C/W	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 81 °C/W.
- The DFN 3x3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

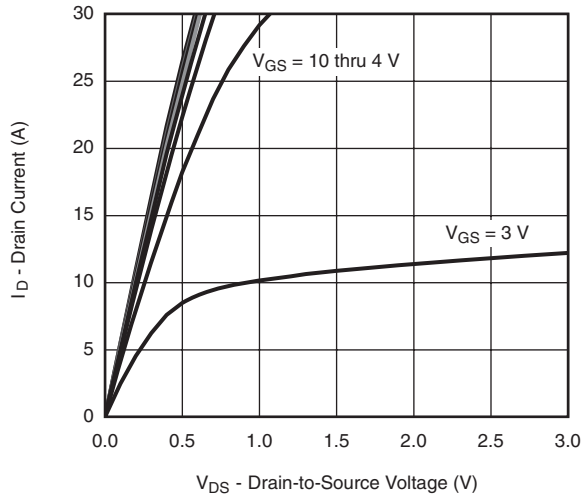
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$		0.021		$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 7.0\text{ A}$		0.025		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 7.8\text{ A}$		17		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		435		pF
Output Capacitance	$C_{oss}$			95		
Reverse Transfer Capacitance	$C_{rss}$			42		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.8\text{ A}$		8	12	nC
				3.8	6	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.8\text{ A}$		1.4		
Gate-Drain Charge	$Q_{gd}$			1.1		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	1.5	3.2	4.5	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			13	20	
Fall Time	$t_f$			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$		12		A
Pulse Diode Forward Current	$I_{SM}$				35	
Body Diode Voltage	$V_{SD}$	$I_S = 6.3\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 6.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	25	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			7	12	nC
Reverse Recovery Fall Time	$t_a$			9		ns
Reverse Recovery Rise Time	$t_b$			6		

Notes:

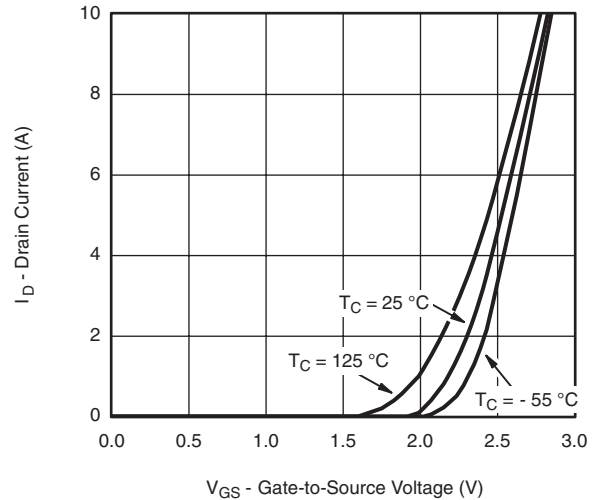
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

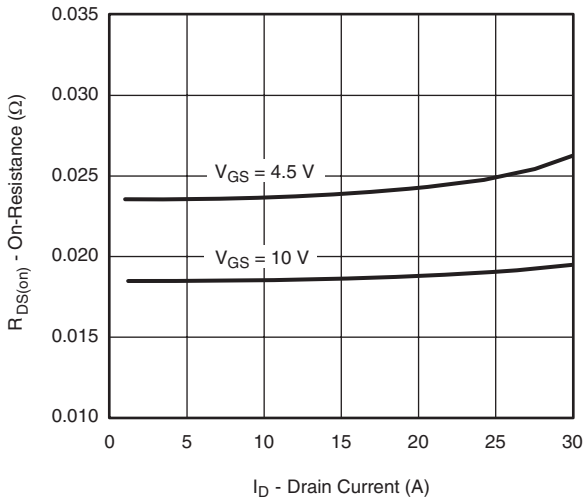
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



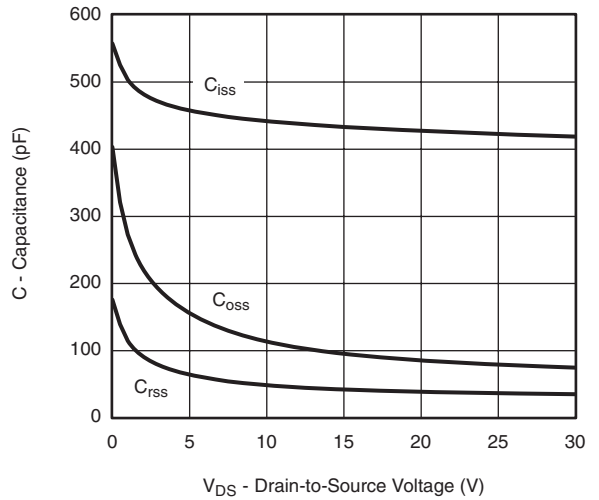
**Output Characteristics**



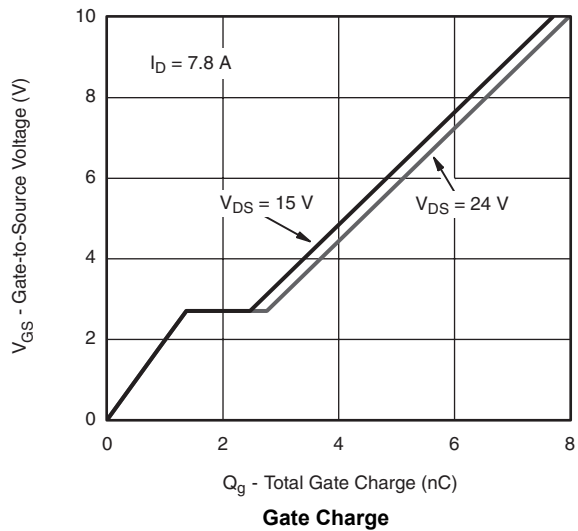
**Transfer Characteristics**



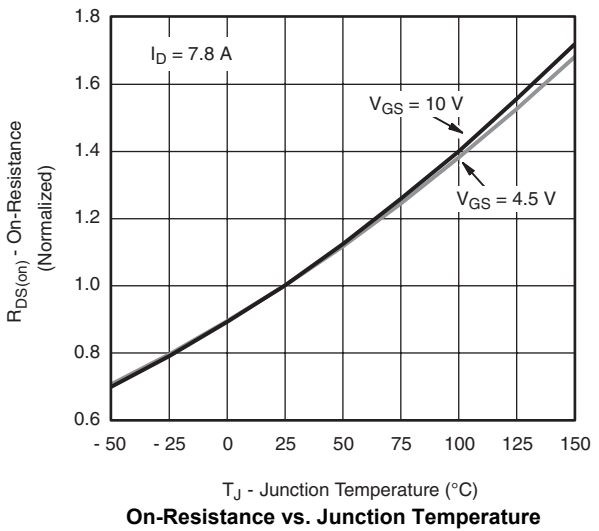
**On-Resistance vs. Drain Current**



**Capacitance**

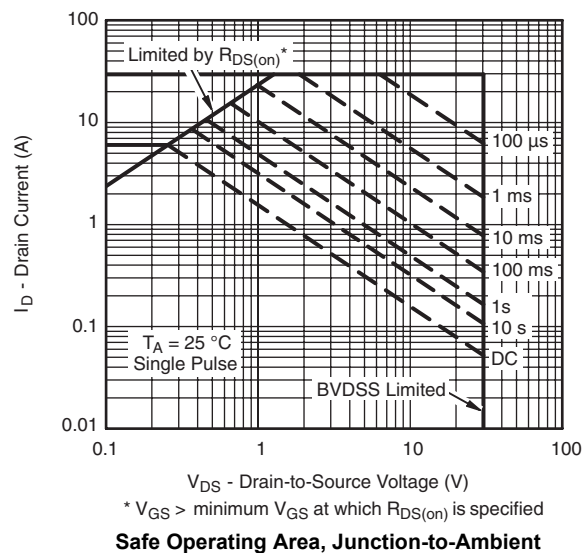
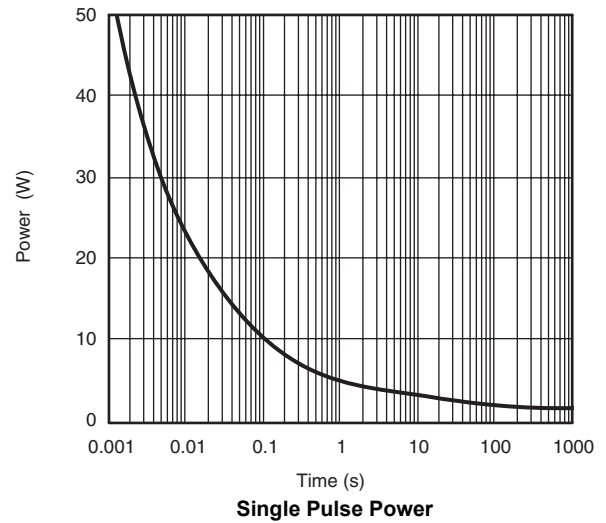
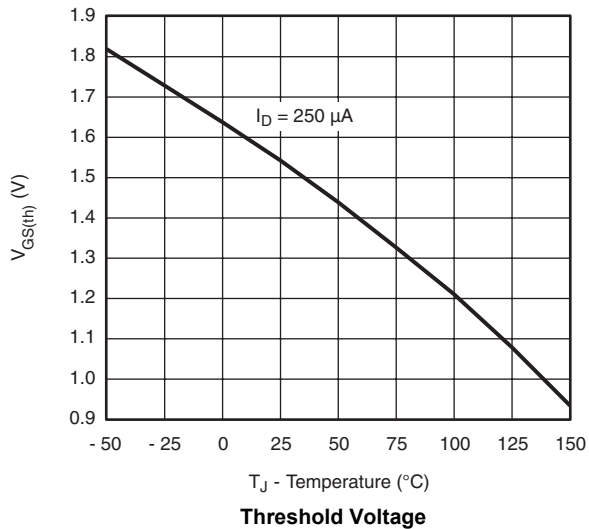
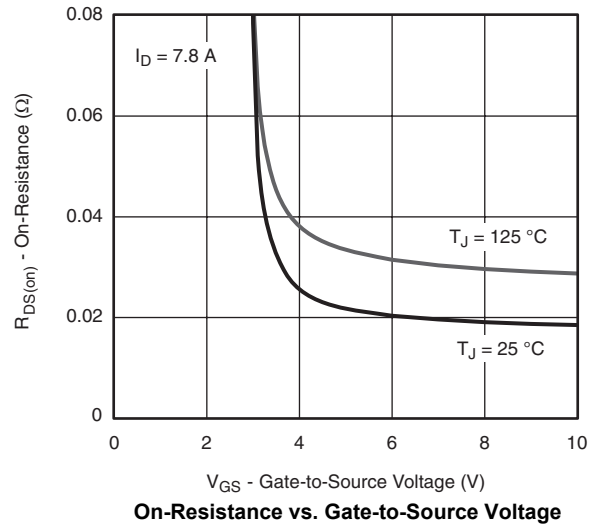
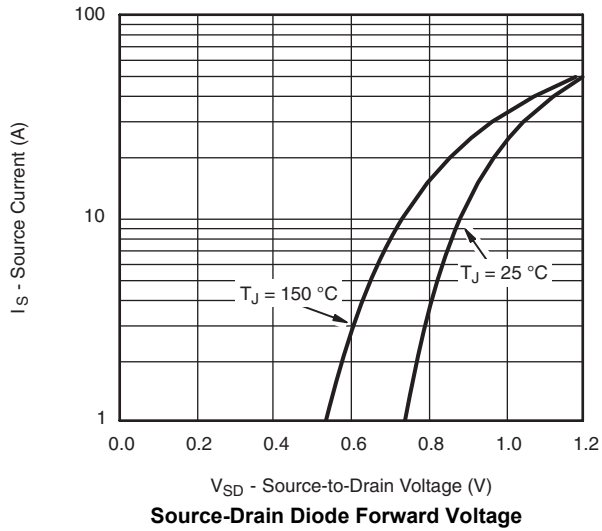


**Gate Charge**

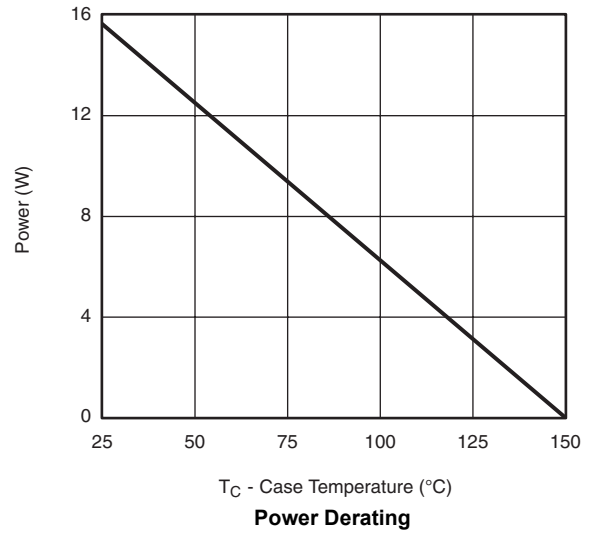
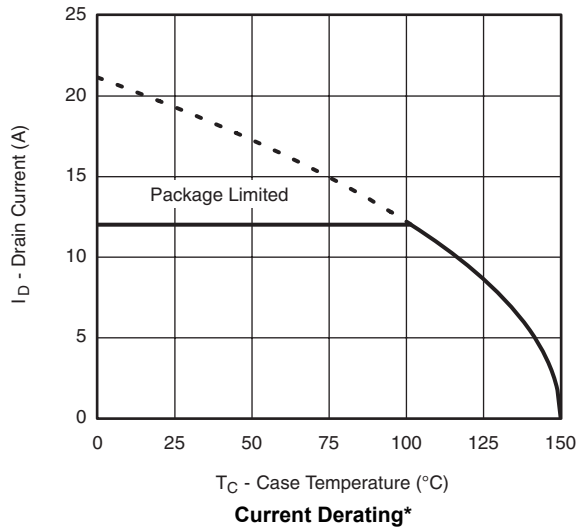


**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

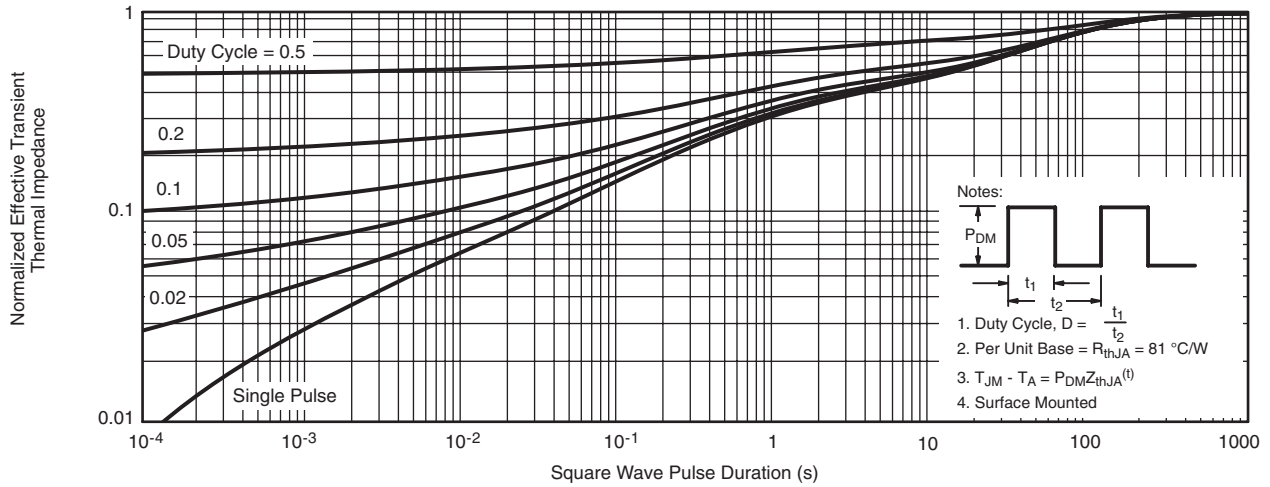


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

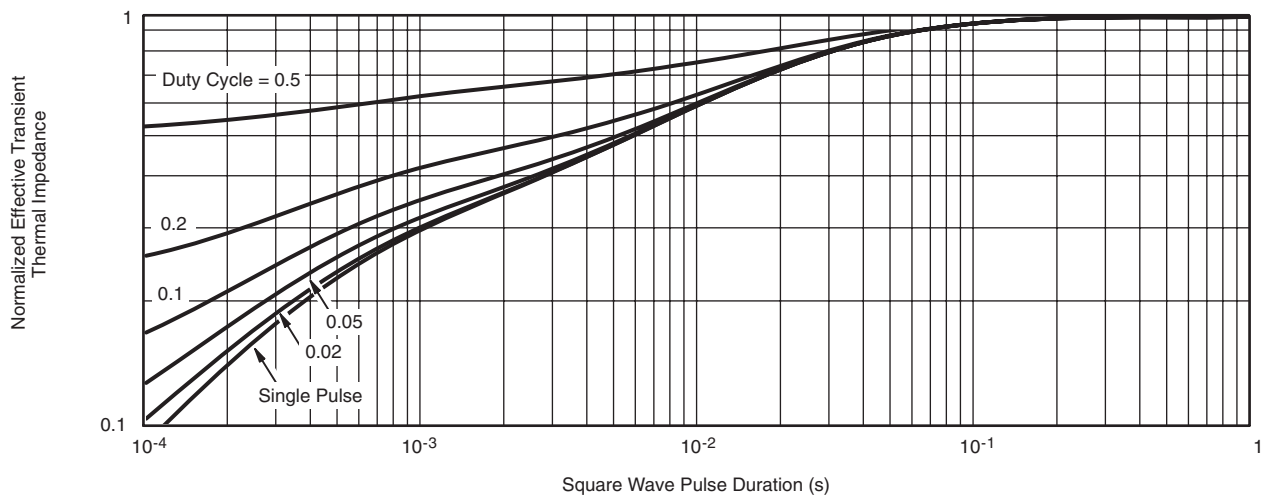


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

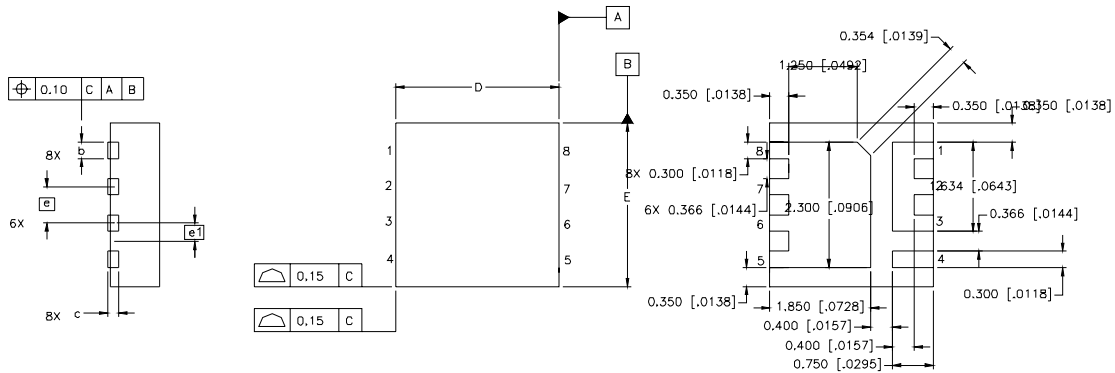


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

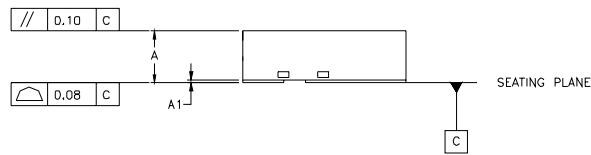
## PQFN Package Details



SIDE VIEW

TOP VIEW

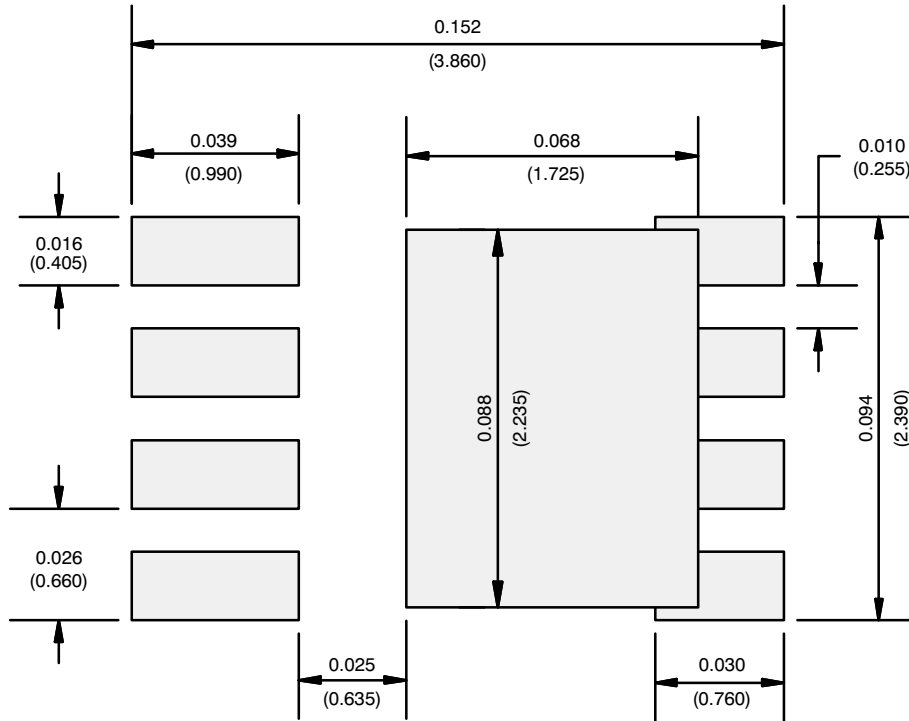
BOTTOM VIEW



FRONT VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0315	.0394	0.800	1.000
A1	.0000	.0020	0.000	0.050
b	.0098	.0138	0.250	0.350
c	.0080 REF.		0.203 REF.	
D	.1181 BASIC		3.000 BASIC	
E	.1181 BASIC		3.000 BASIC	
e	.0262 BASIC		0.666 BASIC	
e1	.0131 BASIC		0.333 BASIC	

RECOMMENDED MINIMUM PADS



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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